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Technical Manual
MAGPAK
SERIAL MAGNETIC TAPE SYSTEM
MODELS 9446/9448

SDS 900647B

October 1965

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GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 SCOPE OF MANUAL

1-3 This manual describes the Model 9446/9448 MAGPAK Serial Magnetic Tape System, which is designed and manufactured by Scientific Data Systems, Santa Monica, California. It includes equipment specifications, operating and programming instructions, theory of operation, installation and maintenance procedures, and detailed drawings of the equipment.

1-4 PURPOSE OF EQUIPMENT

1-5 The MAGPAK Tape System is designed to provide a sequential-access memory device for use with small-to-medium general purpose digital computers. MAGPAK is compact, inexpensive, and simple to operate and maintain. The use of tape cartridges helps eliminate the tape threading problems and sequencing problems inherent with standard magnetic tape, paper tape, and punched card equipment.

1-6 TYPICAL APPLICATIONS

1-7 With MAGPAK, the user can operate a complete library of automatic compilers and assemblers with little manual intervention. Using these automatic programming systems, the four MAGPAK tape tracks are frequently organized as follows:

a. Program library storage (write protected)
b. Temporary storage
c. Object programs
d. Source programs and data or computational results

1-8 PHYSICAL DESCRIPTION

1-9 The MAGPAK Tape System consists of two basic units: the Model 9446 Tape Transport Unit (shown in figure 1-1), and the Model 9448 Tape Control Unit (shown in figure 1-2). From one to four tape transport units can be operated on-line with one tape control unit. Information is stored on two Model 9401 Tape Cartridges. Table 1-1 lists standard and accessory equipment for MAGPAK, and figure 1-2 shows the main system components and accessories.

1-10 MODEL 9446 TAPE TRANSPORT UNIT

1-11 Model 9446 consists of two separate tape stations mounted on a single panel, and an electronics chassis which is physically located behind the transports and is part of the transport unit assembly. The left tape station (viewed from the front) is usually designated tape station number 1; the right, tape station number 2. Each tape station is completely independent; that is, each contains its own motors, control panel, and electronics.

1-12 Each of the two tape stations has two independent data channels. Each data channel has its own tape track, file protect switch, and UNIT SELECT switch. The data channels are designated odd and even. The odd channel controls (i.e., UNIT SELECT and file protect) are on the left side of each transport; the even controls, on the right. The odd data channel on the tape is the one nearer the transport casting; the even data channel is the one nearer the operator.

1-13 MODEL 9448 TAPE CONTROL UNIT

1-14 Model 9448 consists of three MX60 Mounting Cases assembled as a unit and ready to mount in a standard 19-inch relay rack. Each MX60 holds up to 20 standard SDS circuit module cards. Each mounting case is hinged on its mounting bracket and swings out to provide access to the connectors.

1-15 MODEL 9401 TAPE CARTRIDGE

1-16 The Model 9401 Tape Cartridge contains 600 feet of 1/4-inch Mylar-base magnetic tape. Each tape has two independent information tracks with a capacity of 1.5 million 7-bit characters per track (one character has 6 data bits plus 1 parity bit). Thus, the two tape cartridges on each MAGPAK provide four independent information channels with a total storage capacity of six million characters. At a packing density of 200 characters per inch and a tape speed of 7.5 inches per second, the data transfer rate is 1500 characters per second.

1-17 SPECIFICATIONS

1-18 Environmental, operational, and power specifications for MAGPAK are given in tables 1-2, 1-3, and 1-4, respectively. Input/output specifications (signal levels, impedances, timing, etc.) for SDS 900 Series Computers are given in two brochures, SDS 910/920 Input/Output (publication number 64-02-09B), and SDS 925/930/9300 Input/Output (publication number 64-03-14B).

LEFT-ODD (CAN'T READ OK
LEFT-EVEN — OK

Table 1-1. MAGPAK Standard and Accessory Equipment

RIGHT - ODD
CAN'T WRITE

RIGHT - EVEN

Model No.	Description	Part No.
9292	Spare Parts Kit for 9448 (optional)	115658
9293	Spare Parts Kit for 9446 (optional)	115660
9401	Tape Cartridge (standard; 2 furnished per 9446)	107565
9402	Dust-Cover Housing (optional; for 9446 when table-mounted	108856
9403	Tape Cartridge Six-Pack (optional; replaces six 9401's)	114049
9446	Tape Transport Unit (standard)	107636
9448	Tape Control Unit (standard)	107550
92360	Table (optional; for mounting up to two 9446's)	107543

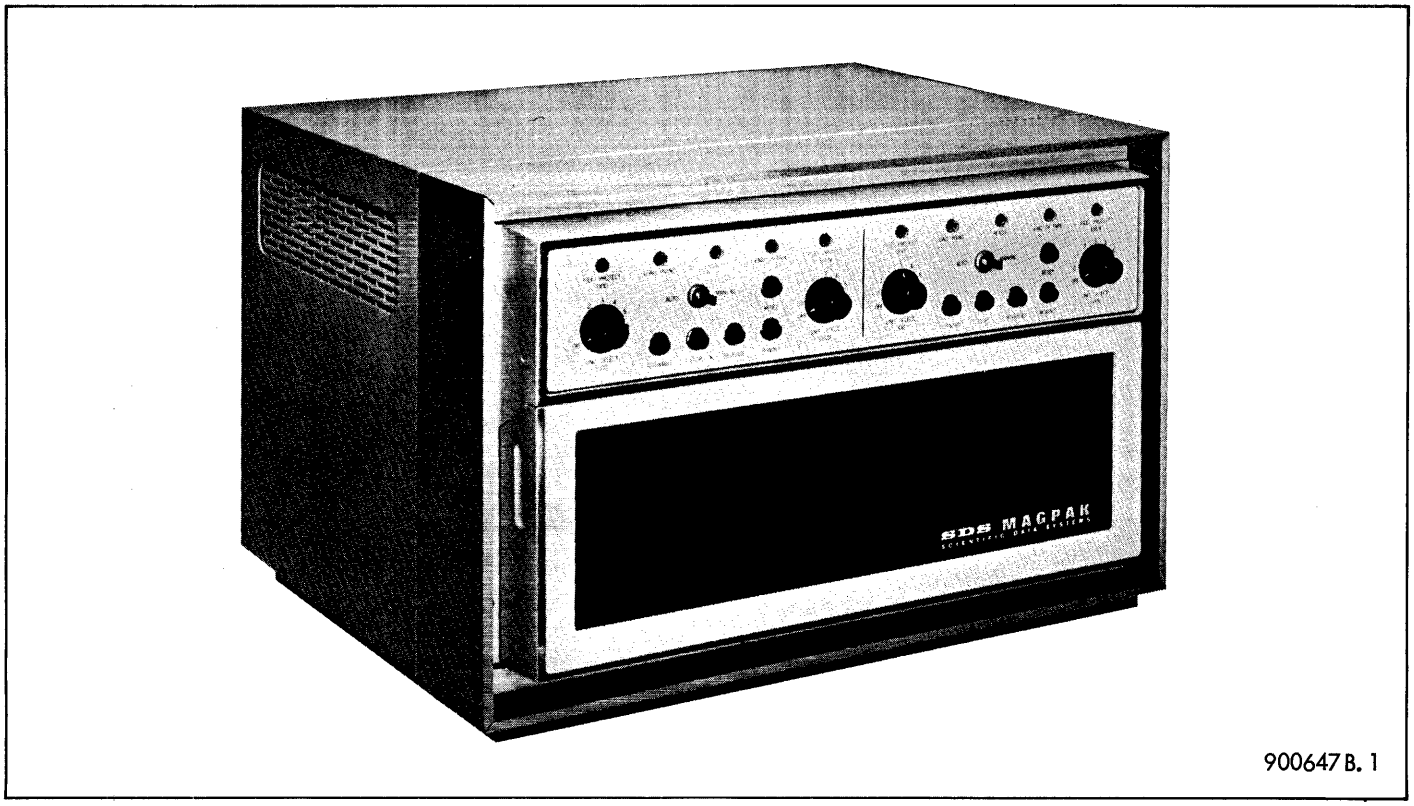


Figure 1-1. MAGPAK Tape Transport Unit

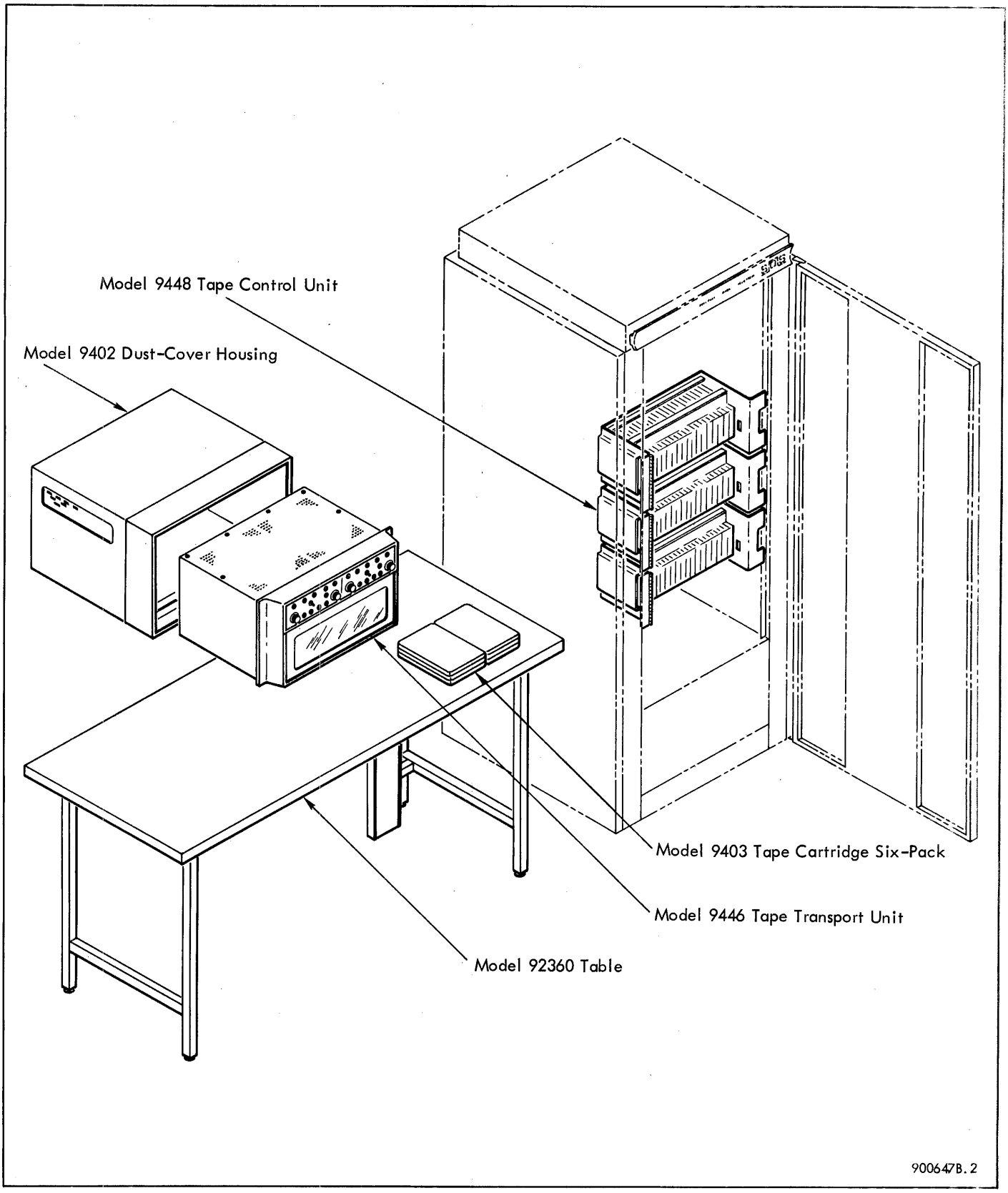


Figure 1-2. MAGPAK System Components and Accessories

Table 1-2. MAGPAK Environmental Specifications

Item	Specification	
	Operating Environment	Non-Operating Environment
Ambient Temperature	10° to 40°C (50° to 104°F)	-50° to +75°C (-58° to +167°F)
Relative Humidity	20 to 80%	0 to 98% (no condensation)
Altitude	0 to 12,000 feet	0 to 40,000 feet
Shock and Vibration	Per commercial data processing installations	Per commercial van and air freight shipments

Table 1-3. MAGPAK Operational Specifications

Item	Specification
Tape Cartridge	SDS Model 9401
Tape Speed (Read/Write)	7.5 ips
Tape Speed (Rewind)	Less than 2 minutes to rewind 600 feet
Tape Drive	Capstan/pressure-roller with mechanical storage
Recording Method	Saturation/frequency doubling
Recording Format	Single channel serial; 6 bits plus parity; self-clocking; 2 channels addressable per tape station
Inter-Record Gap	3/4 inch
Recording Density	1400 bit per inch (200 characters per inch)
Character Read/Write Rate	1500 characters per second
Tape	1/4-inch wide, 600-ft long, 1-mil thick, Mylar base
Read/Write Head	Two-channel, dual gap
Beginning-of-Tape Sensing	Clear section of tape photosensing
End-of-Tape Sensing	Reflective marker photosensing

Table 1-4. MAGPAK Power Specifications

Item	Specification	
	Model 9446	Model 9448
115 vac ±10%, 60 ±3 cps	2.0 amp	
+50 vdc	0.4 amp	
+25 vdc	1.0 amp	3.4 amps
+ 8 vdc	1.6 amps	1.6 amps
-25 vdc	0.2 amp	0.4 amp

1-19 FUNCTIONAL DESCRIPTION

1-20 MAGPAK performs all of the functions of high-speed, IBM-compatible, magnetic tape units, and uses the same instruction set. Programs written for MAGPAK and those written for standard magnetic tape units are identical. The basic difference between MAGPAK and a "big tape" unit is in the method of recording. The high-speed tape unit records seven tracks simultaneously in parallel; MAGPAK records one track at a time, serially.

1-21 A MAGPAK Tape System provides the following features which are also found on the standard high-speed tape systems: binary or BCD coding; recording formats of one, two, three, or four characters per word; a read-after-write check performed on all writing operations; record keys examined without stopping the tape, searching for a given record and detecting end-of-file records in either forward or reverse; each data channel independently file protected.

SECTION II
OPERATION AND PROGRAMMING

2-1 OPERATING INSTRUCTIONS

2-2 CONTROLS AND INDICATORS

2-3 The MAGPAK manual control panel shown in figure 2-1 provides for mode selection, local control of tape motion, and indications of unit status. All tape transport unit controls are interlocked so that no sequencing of control panel switches or commands from the tape control unit will cause damage to the equipment. The indicators correspond to the tape unit status and indicate the tape unit response upon interrogation from the computer.

2-4 AUTO-MANUAL Switch

2-5 The AUTO-MANUAL switch is a two-position toggle switch that is used to select either the automatic or manual mode of operation. In the AUTO position, tape unit functions are controlled by the computer. In the MANUAL position, they are controlled by pushbuttons on the manual control panel. The FORWARD, REVERSE, and REWIND pushbuttons are inoperative in the automatic mode.

2-6 UNIT SELECT Switches

2-7 The UNIT SELECT ODD and UNIT SELECT EVEN switches are nine-position rotary switches that permit the operator to designate numbers 0 through 7 as the unit numbers of the odd and even data channels used in the system. When the system is in the automatic mode, a tape unit will respond only to computer commands whose address bits correspond to its UNIT SELECT switch settings. An OFF position is provided to prevent selection of unwanted channels.

2-8 FORWARD Pushbutton

2-9 The FORWARD pushbutton operates in the manual mode to move tape forward (left to right) at 7.5 ips. Forward tape motion stops when load point is encountered, or when the end-of-tape marker is encountered in the manual mode.

2-10 REVERSE Pushbutton

2-11 The REVERSE pushbutton operates in the manual mode to move tape reverse (right to left) at 7.5 ips. Reverse tape motion stops when load point is encountered.

2-12 REWIND Pushbutton

2-13 The REWIND pushbutton operates in the manual mode to move tape in the reverse direction (right to left) at rewind speed (less than two minutes are required to rewind 600 feet of tape). Rewind motion stops when load point is encountered.

2-14 STOP Pushbutton

2-15 The STOP pushbutton can be used in either the manual or automatic modes to stop tape motion. It directly resets the motion flip-flops.

2-16 RESET Pushbutton

2-17 The RESET pushbutton is used to clear a fault condition or to obtain a ready condition after loading a new tape cartridge. When a tape unit is in a non-ready condition, the capstans do not rotate and (if the unit is in automatic) the READY indicator is not lit. Pressing the RESET button will place the unit in operation.

2-18 FILE PROTECT Indicators

2-19 The FILE PROTECT ODD and FILE PROTECT EVEN indicators are lit when no writing is possible on the odd or even data channels of a particular transport. This means that information on a specified tape track cannot be erased inadvertently. There is a FILE PROTECT indicator for each data channel.

2-20 LOAD POINT Indicator

2-21 The LOAD POINT indicator is lit whenever the tape is positioned such that the beginning-of-tape clear space is being sensed.

2-22 END OF TAPE Indicator

2-23 The END OF TAPE indicator is lit whenever the tape is positioned on or past the end-of-tape reflective marker.

2-24 READY Indicator

2-25 The READY indicator is lit whenever a tape is in automatic and is available for use under computer control. When a tape unit is in use, is in the manual mode, or a fault condition exists, the READY indicator is off.

2-26 TURN ON/TURN OFF PROCEDURES

2-27 Power for MAGPAK is turned on or turned off when the computer cabinet power supply is turned on or off. The MAGPAK tape system has no independent power supply; it uses standard computer power levels. Power sequencing is

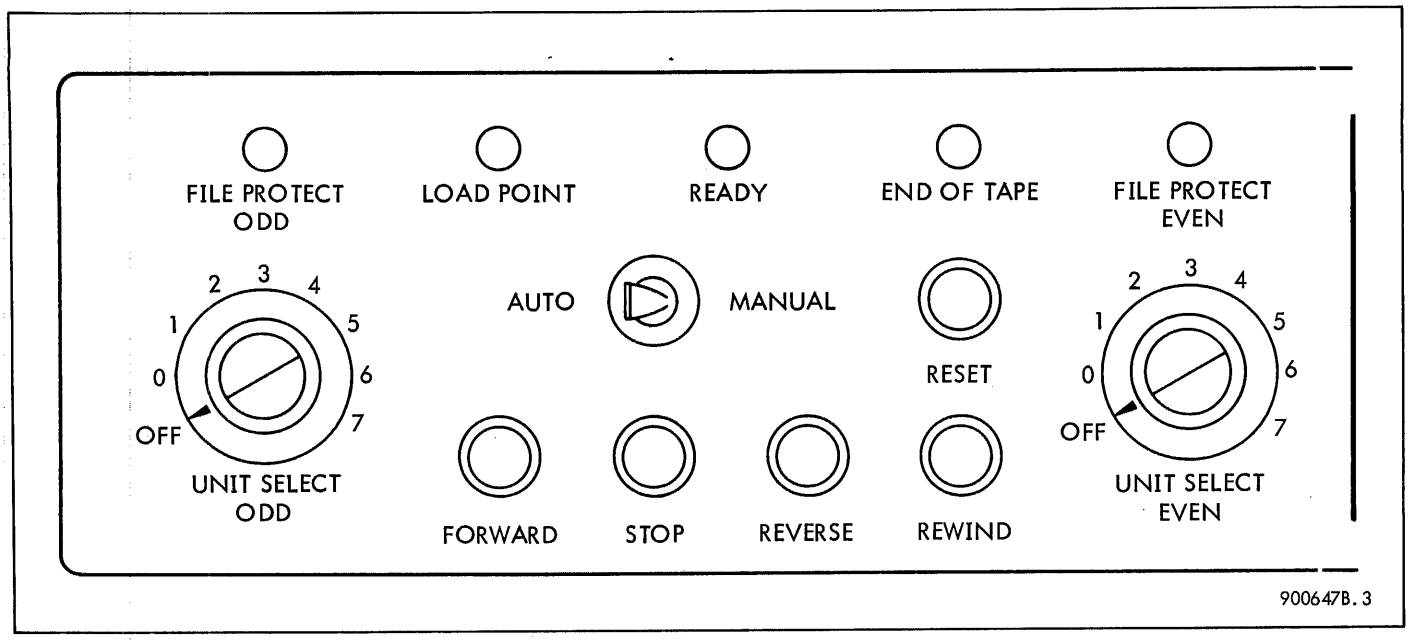


Figure 2-1. MAGPAK Manual Control Panel

self-contained and no detrimental condition will occur under any combination of power sequencing-control panel operation.

2-28 To prepare MAGPAK for operation, refer to figure 2-2 and perform the following steps:

a. Apply power to computer cabinet.

b. Place AUTO-MANUAL switch on control panel in MANUAL.

c. Set UNIT SELECT switches on control panel to the desired unit number setting.

d. Place load lever in LOAD position.

e. Load tape cartridge on transport as explained in paragraph 2-29.

f. Return load lever to RUN position.

g. Press RESET button on control panel.

h. Press FORWARD button on control panel. Tape will run forward to load point and stop.

i. Press FORWARD button again and allow unit to run forward several feet. Press STOP button.

j. Press REVERSE button; tape will stop near the physical beginning of the load point clear space.

k. Place AUTO-MANUAL switch on control panel in AUTO. The READY indicator should light indicating the unit is ready to operate under computer control.

2-29 TAPE CARTRIDGE LOADING PROCEDURE

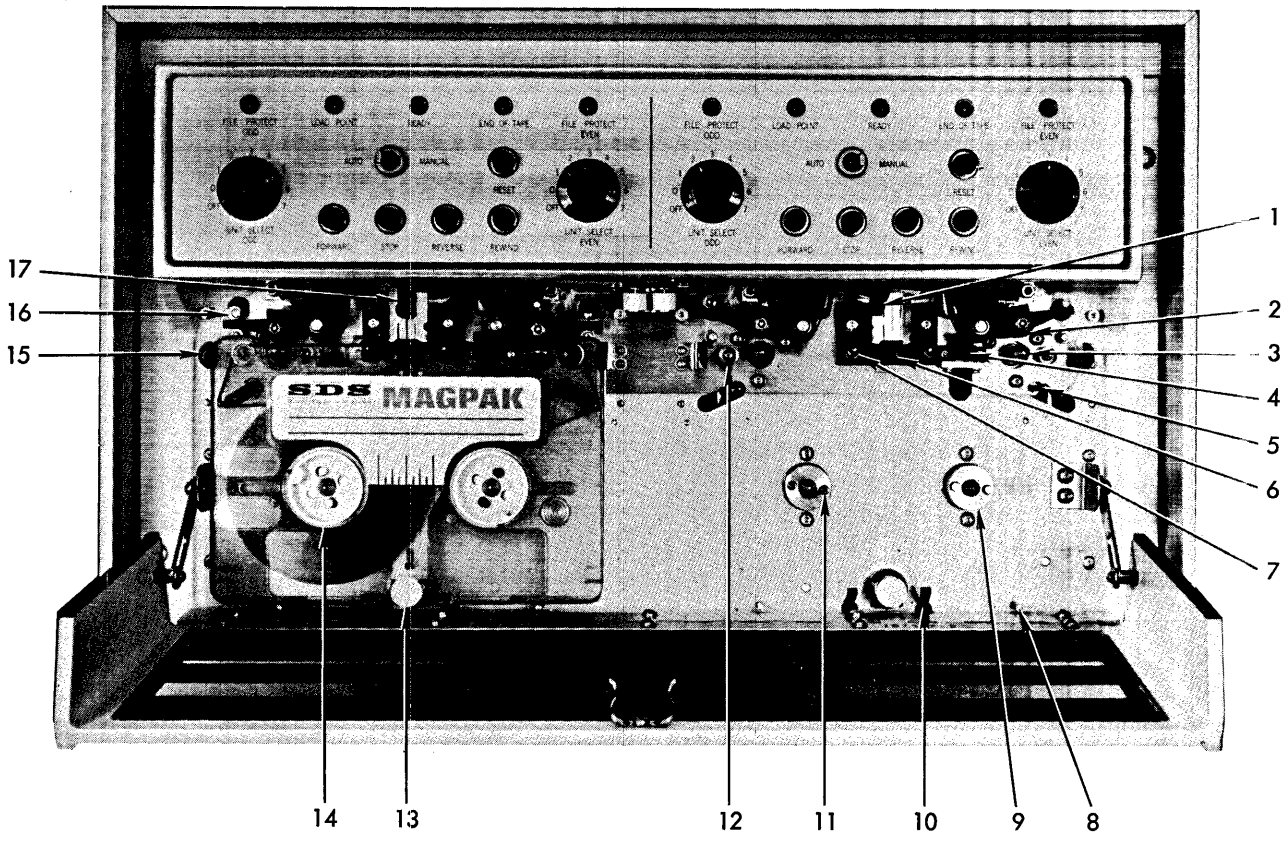
2-30 Proper loading of the tape cartridge will help ensure satisfactory performance of MAGPAK. It is also important that only tape cartridges that conform to SDS Specification No. 108673 be used. The conventional, audio-type cartridges that are commercially available are not controlled to as high a quality standard as are SDS Model 9401 Tape Cartridges. Therefore, it is suggested that Model 9401 cartridges be used.

2-31 If possible, each new cartridge used should be wound to the end and rewound to the beginning to ensure that the tape is winding evenly and is centered on the cartridge reel. If any difficulty is encountered in tape winding, refer to section IV of this manual, "Tape Cartridge Fit Adjustments."

2-32 The tape cartridge should load and unload freely. Tape should not bind on any tape guide surface. The parts which contact the tape during loading (the read/write head, crosstalk shield, head guide pins, capstans, and photosense head) are beveled so that tape should guide into proper position without damage. The pressure-rollers and tension arms are retracted by the load lever during loading so that they clear the tape.

Note

When loading a tape cartridge, be careful not to touch the oxide (upper) surface of the tape. Skin oils or dust on the tape can cause read/write malfunctions. The tape should be fully wound on either reel to prevent marking the data portions of the tape.



1. Load Lever (LOAD Position)
2. Pressure-Roller
3. Capstan
4. Photosense Head
5. Tension Arm Pickup Pin
6. Cross-Talk Shield
7. Head Guide Pin
8. Positioning Pin
9. Reel Motor Hub
10. File Protect Switch
11. Reel Motor Hub Pin
12. Locator Pad
13. Hold-Down Button
14. Cartridge Reel
15. Spring Clip
16. Tension Arm Stop Pin
17. Load Lever (RUN Position)

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Figure 2-2. MAGPAK Tape Cartridge Loading Hardware

2-33 See figure 2-2 for identification of transport hardware associated with loading and unloading. To load the tape cartridge, perform the following steps:

a. Move load lever clockwise to load detent (LOAD position).

b. While holding cartridge in hand, rotate cartridge reels to tighten tape between reels.

c. Place notch in bottom of cartridge over nylon hold-down button shaft at bottom of transport; push cartridge down so that shaft slides into notch. Downward motion will stop when cartridge contacts the two positioning pins located on either side of the hold-down button.

d. Maintaining a downward pressure on cartridge to keep it against positioning pins, push the top forward between the spring clips until it snaps "home" against locator pads. Cartridge must be seated firmly against locator pads.

e. Move load lever counterclockwise to RUN position.

f. Rotate cartridge reels by hand slightly so that reel motor hub pins engage cartridge reels. There are two pins per hub; both must be engaged or tape will not wind properly. The tape cartridge is now ready to operate.

2-34 TAPE CARTRIDGE UNLOADING PROCEDURE

2-35 It is very important that the tape be run to the physical beginning-of-tape before the cartridge is removed from the transport. This ensures that any tape damage that might have occurred during loading or unloading of a cartridge will be confined to the section of tape between the load point marker and the physical beginning-of-tape. This section of tape is not used for information storage.

2-36 See figure 2-2 for identification of transport hardware associated with loading and unloading. To remove a cartridge from the transport, perform the following steps:

a. Run tape to physical beginning-of-tape and stop.

b. Move load lever clockwise to LOAD position.

c. Pull top of cartridge away from transport and lift cartridge out of hold-down apparatus.

2-37 PLACEMENT OF FILE PROTECT (WRITE) PLUGS

2-38 If a data channel is to be file protected, then a write plug (SDS 108784) should not be inserted between the file protect switch lever and the bottom of the tape cartridge. Conversely, if a data channel is to be written on, then a write plug should be inserted in the cartridge corresponding to the channel to be written. To enable writing on the odd channel, insert a write plug in the bottom left cavity of the cartridge (viewed from the front); to enable writing on the even channel, insert a write plug in the bottom right cavity of the cartridge.

2-39 PLACEMENT OF LOAD-POINT CLEAR SPACE AND END-OF-TAPE MARKERS

2-40 As shown in figure 2-3, a reflective marker strip is placed on the non-oxide surface of the tape approximately 14 feet from the end of the reel to indicate end-of-tape. IBM 352407 Reflective Tape, or equivalent, should be used for this marker. A clear section of tape (one with the oxide removed) is located approximately 30 inches from the beginning of the reel to indicate load-point.

2-41 PROGRAMMING

2-42 INTRODUCTION

2-43 The basic programming to write or read information on any magnetic tape device (including MAGPAK) is essentially the same as for any input/output device with or without interlace control. However, magnetic tape in general (and MAGPAK in particular) is also used as an external storage device rather than strictly an input or output device. Therefore, certain functions which are unique to programming for magnetic tape systems are presented in detail in this section. Note that all functions that can be performed on a standard high-speed tape unit (such as SDS Model 9248) can be performed on MAGPAK.

2-44 Without-Leader EOM Instructions

2-45 As a general rule, all EOM instructions to the tape units should specify start-without-leader. Since the tape unit generates gap on all write operations automatically, it is not necessary for the starting EOM to call for leader. A leader instruction should never be included in a magnetic tape program because the buffer will then attempt to generate leader, and an erroneous operation may occur.

2-46 Four-Character Mode

2-47 As a general rule, tape units should be programmed for four characters per word if possible. (The write-tape-mark operation is an exception to this rule.) It is possible to write tape in a 1-, 2-, or 3-character-per-word mode provided the buffer can be kept supplied with characters at a sufficient rate. On reading, however, the tape unit uses the buffer character count to ascertain when it has read two characters and can look for gap. If a 1-character-per-word read were started, a single noise character would stop the tape. All scan operations must be in 3- or 4-character-per-word mode or the tape will not stop when it reaches gap.

2-48 Timing Considerations

2-49 The Tape Control Unit is designed such that there are no timing restrictions on programming the tape unit. The programmer need only concern himself with ascertaining that the unit is ready before he gives a start command.

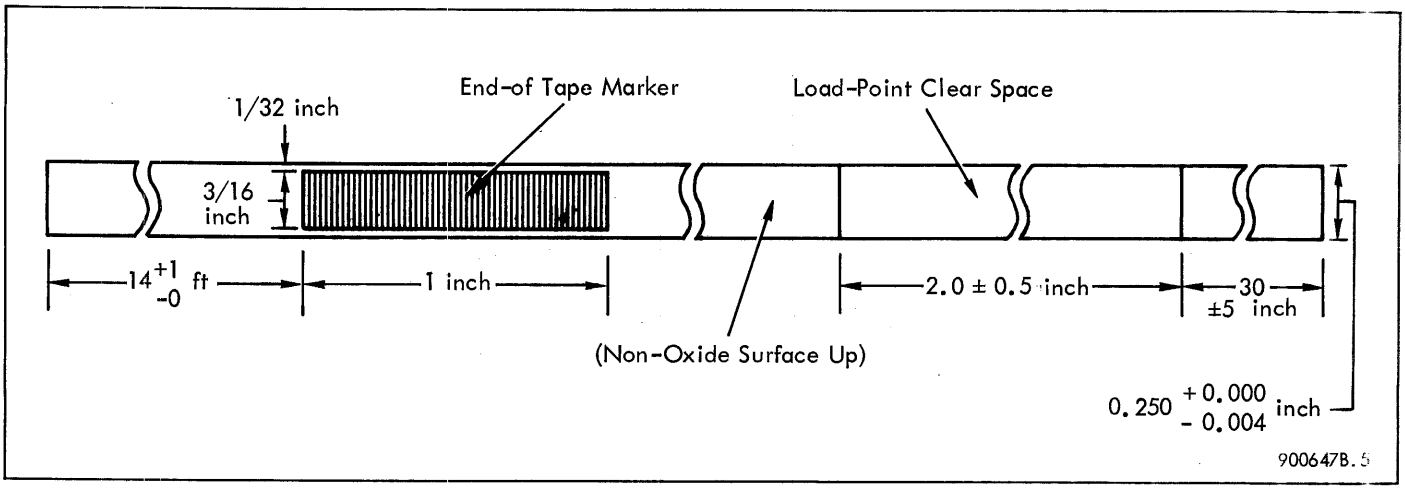

Figure 2-3. Location of Load-Point Clear Space and End-of-Tape Marker

2-50 Longitudinal Check Character

2-51 No longitudinal check character, per se, is written. However, when writing in a 1-character-per-word mode, the character is written twice in order to detect the file mark character (1717).

2-52 Buffer Ready Indication

2-53 When programming the tape unit without using the interrupt system, the user should allow the buffer to become ready after the completion of a tape operation before starting another operation. This is necessary because, even though the tape unit itself is physically ready, the tape control unit and buffer are busy for as much as 64 microseconds longer. The tape control unit must signal the buffer that the operation is complete, and the buffer must then disconnect the tape control unit.

2-54 In general, when programming two or more tape operations sequentially, the buffer ready signal is used to determine when the first operation is complete, and then the tape unit ready signal is used to determine if the second operation can be initiated. Continued operations are an exception to the rule. In a continued operation, the tape is kept moving; therefore, it is never ready.

2-55 Reading Beyond the Last Write

2-56 Once the programmer has written a record on tape, he cannot be assured that any records after that can be read. This means that a record in the middle of a file cannot be updated or rewritten if the user ever wishes to read the records that follow it.

2-57 Backspace or Rewind After a Write

2-58 An end-of-file character should be written, or a segment of tape erased after a series of records have been written, if the user wishes to backspace or rewind and then expects to return at some later time to record additional information at the end of the previous series of records. This practice provides positive identification of the end of a record and facilitates return to a specific location on the tape. If this method is not used, there is a possibility that the tape will not stop in the same location at the end of the series of records as it did when the last record was written. This would leave a segment of tape in the gap which has not been written and may cause erroneous operation when the tape is read.

2-59 TAPE TRANSPORT UNIT STATUS SIGNALS

2-60 The tape transport unit sends ten status signals to the computer which can be tested with SKS instructions as described in the following paragraphs. These may be tested at any time to determine the status of a tape unit or data channel.

2-61 Tape-Unit-Ready Test

2-62 The tape-unit-ready test, TRT (SKS 10410 for unit 0 on the W-buffer), will skip if the tape unit is not ready. Test instruction TRT may be used with two BRU instructions to wait for the tape unit to become ready before starting an operation. The tape unit is not ready if at least one of the UNIT SELECT switches on the tape units in the system is not set to the logical unit number being tested, or if the unit is not in automatic mode of operation. If the tape on the selected unit is in motion for any operation, the unit will not be ready.

2-63 File-Protect Test

2-64 The tape file-protect test, FPT (SKS 14010 for unit 0 on the W-buffer), will skip if the file protect is not on. In other words, if the tape can be written, the FPT instruction will skip; if it cannot be written, FPT will not skip. This instruction should be used before any write operation to ascertain if it is possible to perform the write.

2-65 Beginning-of-Tape Test

2-66 The beginning-of-tape (or load-point) test, BTT (SKS 12010 for unit 0 on the W-buffer), will skip if the tape is not positioned at load point. This instruction can be used to determine when or if the tape is rewound.

2-67 End-of-Tape Test

2-68 The end-of-tape test, ETT (SKS 11010 for unit 0 on the W-buffer), will skip if the tape is not at the end-of-tape marker. It should be used after every write operation to determine when the end-of-tape is reached.

2-69 Density Tests

2-70 MAGPAK always responds 200 bpi to a density test interrogation. It will not skip on the 200 bpi test, DT2 (SKS 16210 for unit 0 on the W-buffer). It will always skip on the high-density tests, DT5 (SKS 16610 for unit 0 on the W-buffer) and DT8 (SKS 17210 for unit 0 on the W-buffer). "Big tape" units on the same channel will test in the normal manner.

2-71 End-of-File Test

2-72 Tape end-of-file test, TFT (SKS 13610 for all tape units on the W-buffer), will not skip if the tape read or scan operation last completed did not encounter a tape mark. The Tape Control Unit will detect a recorded tape mark and signal end-of-file after any read or scan operation in either the forward or reverse direction. This signal should be tested until the completion of the operation because the end-of-file signal will be true until some character, other than the tape mark, is read. The end-of-file test is a Tape Control Unit signal, rather than a Tape Transport Unit signal. Therefore, any unit address may be used to test the control unit.

2-73 Gap Test

2-74 The tape gap test, TGT (SKS 12610 for any tape on the W-buffer), will skip as long as the tape is not in motion in the gap following a record written or read. When the tape unit has detected the gap at the end of a record, it will generate the gap signal. This signal will remain true for approximately ten milliseconds. During this time, the test instruction will not skip and the tape may be given a command to continue in the direction it is going. If so programmed, the tape will continue without stopping.

2-75 If the record encountered should be an end-of-file, the gap signal will not become true, and the tape will always stop. Like the end-of-file test, the gap test is a control unit test and any tape unit address may be used.

2-76 Skip If Not MAGPAK

2-77 The skip if not MAGPAK test MPT (SKS 1021n) skips if the selected unit is not MAGPAK.

2-78 WRITING

2-79 Introduction

2-80 Writing on magnetic tape is essentially the same as outputting information to any other output device, with or without the interlace to control data transfer. The program should first determine that the desired logical unit is ready and that the file protect is off. Interlace may be controlled, then set up, and the write-tape-binary (WTBW or WTBY) is executed. The interlaced buffer then governs transfer of data to the tape. A typical binary start-write sequence, with tape unit No. 6 connected to the W-buffer, is shown in table 2-1.

Table 2-1. Binary Start-Write Sequence

Memory Location	Instruction Code	Mnemonic	Remarks	
01000	0 02 50000	EOM* START	10000	Alert the interlace
01001	0 02 10000	EOM	10000	Set two high-order count bits
01002	0 13 01040	POT CW		Send control word to interlace
01003	0 02 03656	WTBW	6, 4	Start write
01040	20004000	OCT CW	20004000	Control word, 256 words starting at 4000

*The EOM in location 1001 is not needed to write a record of 256 words, but is there merely to illustrate the general case.

2-81 The buffer will automatically terminate its output when the interlace word count is reduced to zero. If the interrupt system is enabled, an I2 (33 or 32) interrupt will be generated when the tape is stopped.

2-82 Write Errors

2-83 If the read-after-write check finds a character parity error, the buffer error flip-flop is set and can be tested with a BET instruction (SKS 20010 for the W-buffer). If there was an error detected on writing, the program should erase backward over the record, then space backward over the

previous record. The previous record is spaced over in a forward direction (or read) and then a rewrite of the previous record may be attempted.

2-84 If the second attempt is also in error, an erase backward – space backward over previous record – space forward over previous record – erase bad section of tape – rewrite routine should be executed. The procedure is continued until the record is correctly written. An erase backward – attempt rewrite routine is not recommended.

2-85 Long-term speed variations can cause the write head to be mispositioned such that the block is not completely erased or the previous inter-record gap is shortened each cycle. Both conditions can cause a tape to be written such that subsequent reading cannot be accomplished.

2-86 A space backward – attempt rewrite routine is not recommended since the write error may have been caused by gap-in-data. A spacing backward sequence could terminate from the gap-in-data location instead of the beginning of record. This may also have the result of not being able to read the information.

2-87 Writing From the Load Point Marker

2-88 It is desirable to erase approximately 3 to 3.5 inches of tape before writing the first record when the tape is situated at the load point. An erase operation for 150 words will clear the desired section. This procedure is particularly important if the previous recording history of the cartridge is unknown.

2-89 Writing Near the End of Tape

2-90 About 14 feet of tape is usually reserved between the end-of-tape marker and the physical end of tape. This space contains at least 12 feet of usable tape. When the end-of-tape marker is sensed, there is sufficient tape remaining to record 28,800 characters.

2-91 End-of-File Definition

2-92 An end-of-file record is defined as a tape mark character 1717. The end-of-file is detected by reading the tape mark. An end-of-file is used to indicate the end of a group of related records or the end of recorded information on a tape.

2-93 Writing the Tape Mark

2-94 The tape mark is a 1-character BCD record regardless of the parity of the previous information on the tape. (Actually, MAGPAK always writes in binary, regardless of the command given. The file mark is written in BCD in order to maintain program compatibility with standard magnetic tape systems.) To start the write process, an EOM instruction for one character per word in BCD should be given. This is followed by an MIW instruction to load a word into the buffer which contains 17XXXXXX (the 17 is the tape mark). The MIW is followed by a terminate output. As in any write operation, when the buffer is ready or when the I2 interrupt occurs, the operation is complete. For example, to write a tape mark on tape unit 3, the sequence in table 2-2 should be used

Table 2-2. Tape Mark Write Sequence

Memory Location	Instruction Code	Mnemonic	Remarks	
02000	0 02 02053	WTDW START	3, 1	Write 1 character/ word, BCD
02001	0 12 02100	MIW	TMC	Output tape mark constant
02002	0 02 14000	TOPW		Terminate output
02100	17000000	OCT TMC	17000000	Tape mark constant

2-95 ERASING

2-96 Introduction

2-97 The erase tape operation is essentially equivalent to writing information except that no data are recorded on tape. The erase is timed like a write operation in that the interlace (or equivalent) is used to supply dummy characters to the buffer and allows the tape unit to clock the desired number of character times for the length of tape to be erased.

2-98 Erasing a Record After a Write Error

2-99 When a write error occurs, an erase in reverse should be used to back up to the beginning of the record. This is accomplished by setting up the interlace (or equivalent) exactly as was done for the preceding write operation, and executing an erase tape reverse, ETRW or ETRY (EOM 07670 for unit 0 on the W-buffer). Termination of the erase is the same as that for a write; when the operation is complete, an I2 (33 or 32) interrupt occurs and the buffer is ready.

2-100 If a record cannot be rewritten, the user should erase it completely and try again on a new section of tape. This is accomplished by first erasing in reverse to the beginning of the record, and then erasing forward for the same number of words as was programmed for the original write or reverse erase. This is programmed the same as a reverse erase except that a normal erase tape instruction, ETW or ETY (EOM 06670 for unit 0 on the W-buffer) is used.

2-101 Erasing a Given Length of Tape

2-102 To erase a fixed section of tape, it is only necessary to calculate the number of words that must be sent to the buffer to clock the erase operation over the desired legnth of tape. An allowance of about 0.45 inch should be made for gap that will be written by the tape control unit automatically. A write or erase operation stops when the read head finds the gap at the end of a record. Since the read head is always reading the gap in an erase operation, the tape stops 0.3 inch shorter after forward erase than after a write operation of the same length.

2-103 READING

2-104 Introduction

2-105 Reading from magnetic tape is similar to reading from paper tape. When the tape is ready, a sequence like the one described for magnetic tape writing is executed, except with a read tape rather than a write tape EOM instruction. The tape will start and the interlace (if used) will store information in memory as the buffer fills. When the gap is encountered, the gap signal will come true; if another read tape command is given, the tape will continue without stopping. If no second EOM is given, the tape will stop, the buffer will become ready, and an I2 (33 or 32) interrupt will be generated. The program may then inspect the error indicator in the buffer to determine if a parity error occurred. If an error did occur, then the program should backspace over the record and attempt to reread it. At least 9 reread attempts, for a total of 10 read tries, should be made before the record is considered bad or unreadable. Usually one reread will suffice to read the record correctly.

2-106 Long Records

2-107 If the record is longer in number of words than the word count set in the interlace, the interlace will reach zero before the gap is detected. When the interlace goes to zero, it disengages its control of the buffer and allows normal program control to resume. When the buffer fills again, an I1 (31 or 30) interrupt will occur. The programmer can choose several responses to this condition. Usual procedure would be to execute a skip-remainder-of-record EOM (SRRW, 02 13610), empty the buffer with a WIM, then clear the interrupt and return to the main program to await the end of record. If, however, the user wishes to continue to read the remainder of the record, he may reload the interlace and allow it to control the reading of the remaining information.

2-108 Reading an End-of-File

2-109 The tape control unit will not generate the gap signal or an I1 interrupt if the program starts the tape in a read operation and the next record is an end of file. The tape will stop, the buffer will become ready, an I2 interrupt is generated, and the end-of-file test will not skip (TFTW, 40 13610). A BCD record which consists only of 17_8(001111) characters will be considered an end-of-file.

2-110 Reading at the End of the Tape

2-111 As in writing, when the end-of-tape marker is encountered, the end-of-tape test will not skip. The user will normally have an end-of-file record after the last recorded information, even if this occurs beyond the end-of-tape marker. If preferred, however, it is possible to use the end-of-tape marker to indicate the end of information.

2-112 SCANNING AND SEARCHING

2-113 Introduction

2-114 The scan-tape operation is like a non-interlaced read operation except that only one I1 interrupt (buffer full condition) occurs for each record. This occurs when the gap is first encountered and while the tape is still moving. The buffer at that time will contain the last four characters of the record. When scanning forward, this means the last word of the record. When scanning reverse, this means the first word of the record which will be in reverse order by characters. For example, if the first word contained the eight octal digits 01 23 45 67, when this is loaded into the buffer in the reverse scan, it would appear as 67 45 23 01. The position of bits in the character is not modified, only the order of the characters is changed in the word.

2-115 Continued Scan

2-116 Since the I1 interrupt (31 or 30), or buffer full condition, occurs when the gap is reached (but while the tape is still moving), it is possible to give another scan instruction and have the tape continue to scan the next record without stopping. The user has 500 milliseconds from the time of the interrupt to give the continue command to keep the tape in operation. If no instructions are received by the tape control unit during this period, it will bring the tape to a stop in the middle of the gap and generate an I2 interrupt. The tape unit and buffer will then be in ready status.

2-117 Reverse Search

2-118 Searching for a given record that is identified by the first word is a simple application of the repeated scan-reverse operation. First, the identifier word should be reversed by character. When the selected tape unit is ready, it is started in reverse scan, SRBW (EOM 07635 for tape unit 5 on the W-buffer). The program may wait for the I1 interrupt, or may be suspended on a WIM instruction until the gap is reached and the buffer is filled with the first word of the record. This word is then compared with the reversed identifier for which the search is being made. If they are not equal, the program gives another scan-reverse EOM and waits to check the next record. If they are equal, the program does not give any further EOM instructions but merely waits for the I2 interrupt or for the

buffer to be ready. The program may then indicate a forward-read, if desired.

2-119 Forward Search

2-120 A search-forward operation could be executed in the same manner as the reverse search if the identifier word was recorded at the end of a record, as well as at the beginning. Since this process is somewhat awkward, provision has been made to search forward on the first word of a record and read the information when the desired record is found. This can be easily implemented since the time between words is on the order of 320 cycles (for 8 μsec cycle time computers).

2-121 The search is accomplished by starting the tape in a forward-read operation, and waiting for the first I1 interrupt (buffer full condition). When this occurs, the identifier word can be compared with the first word of the record. If they are not equal, an RTSW instruction (EOM 1400X for tape units on the W-buffer) is given to convert the read operation to scan. When the next I1 occurs, the tape is at the end of the record, and the program may give another read EOM to keep the tape moving and check the next record. If the identifier word and the first record word are equal, the program may go ahead and read the record, either under program control or by setting the interlace.

2-122 Scanning an End-of-File Record

2-123 As in the read mode, when an end-of-file record is encountered while scanning, the end-of-file test will not skip. In the scan mode, however, an I1 interrupt will occur after the end-of-file record is encountered and before the tape stops.

2-124 Scanning Near the Beginning of Tape

2-125 When scanning in reverse, the detection of the load-point marker will cause the tape to be stopped and an I2 (33 or 32) interrupt and buffer ready condition to occur. This is the only time in the scan mode of operation that an I2 interrupt occurs without prior occurrence of an I1 interrupt.

2-126 Scanning Near the End of Tape

2-127 The end-of-tape detection causes no special action other than the setting of the end-of-tape signal. If the end of information is not indicated by an end-of-file record, the program should check the end-of-tape signal before scanning forward over the next record.

2-128 SPACING

2-129 Space Forward or Reverse, One Record

2-130 To space one record, the tape is started forward (or reverse, as desired) in a scan mode and the program waits for the buffer to be ready or for the I2 interrupt. The I1 interrupt should be ignored by executing a WIM instruction to a dummy location, and then executing the BRU indirectly to clear the interrupt channel. When the I2 interrupt occurs, or when the buffer is ready, the tape will have been stopped in the gap following the record over which the space was executed.

2-131 Space More Than One Record

2-132 To space more than one record, another scan EOM instruction should be executed when the I1 interrupt occurs indicating the detection of gap. This may be repeated until the desired number of records have been spaced over. The end of file, however, will require special consideration when spacing over a file of unknown length. The user may wish to program a check for end of file when spacing.

2-133 REWINDING

2-134 A tape unit may be started in rewind at any time as long as the unit is ready. This operation does not use the buffer or the tape control unit. Any or all tape units may be rewound while any input/output operation (on tape units or other devices) is in progress. The rewind instruction, REWW, is an EOM (02 14016 for tape unit 6 on the W-buffer). Once started, the tape will continue in rewind until the beginning of tape is sensed. It will then stop.

2-135 SUMMARY OF TAPE OPERATION CODES

2-136 Tables 2-3 and 2-4 contain a summary of operation codes used with the MAGPAK tape system.

Table 2-3. Test Conditions

Mnemonic	Description	Buffer	Coding
TRTW n TRTY n	Skip if tape unit n is not ready	W Y	SKS 1041n SKS 1051n
FPTW n FPTY n	Skip if tape unit n not file-protected	W Y	SKS 1041n SKS 1411n
BTTW n BTTY n	Skip if tape unit n not at beginning of tape	W Y	SKS 1201n SKS 1211n
ETTW n ETTY n	Skip if tape unit n not at end of tape	W Y	SKS 1101n SKS 1111n
DT2W n DT2Y n	Skip if tape unit n not at 200-bpi density	W Y	SKS 1621n SKS 1631n
DT5W n DT5Y n	Skip if tape unit not at 556-bpi density	W Y	SKS 1661n SKS 1671n
DT8W n DT8Y n	Skip if tape unit not at 800-bpi density	W Y	SKS 1721n SKS 1731n
TFTW TFTY	Skip if not end of file	W Y	SKS 13610 SKS 13710
TGTW TGTY	Skip if not gap	W Y	SKS 12610 SKS 12710
MPTW MPTY	Skip if unit not MAGPAK	W Y	SKS 1021n SKS 1031n

Table 2-4. Tape Functions

Mnemonic	Description	Buffer	Coding
WTBW n, 4 WTBY n, 4	Write in binary on tape unit n, 4-characters per word	W Y	EOM 0365n EOM 0375n
ETW n, 4 ETY n, 4	Erase tape on tape unit n (Binary or BCD has no effect on erase)	W Y	EOM 0367n EOM 0377n
ETRW n, 4 ETRY n, 4	Erase tape reverse on tape unit n 4-characters per word	W Y	EOM 0767n EOM 0777n
RTBW n, 4 RTBY n, 4	Read in binary on tape unit n	W Y	EOM 0361n EOM 0371n

Menemonic	Description	Buffer	Coding
SFBW n, 4 SFBY n, 4	Scan forward in binary on tape unit n	W Y	EOM 0363n EOM 0373n
SRBW n, 4 SRBY n, 4	Scan reverse in binary on tape unit n	W Y	EOM 0763n EOM 0773n
REWW n, 4 REWY n, 4	Rewind tape unit n	W Y	EOM 1401n EOM 1411n
RTSW RTSY	Convert read to scan (same instruction as terminate output, TOPW or TOPY)	W Y	EOM14000 EOM14100
SRRW SRRY	Skip remainder of record	W Y	EOM 13610 EOM 13710

SECTION III
THEORY OF OPERATION

3-1 INTRODUCTION

3-2 Contained in this section is a description of the electromechanical, functional, and logical theory of operation for MAGPAK. In general, the first part of this section deals with the 9446 Tape Transport Unit, and the second part with the 9448 Tape Control Unit. A list of logic equations and a glossary of logic terms for both units are included at the end of this section. Logic diagrams and other reference drawings are included in section V of this manual.

3-3 MAGPAK CODING SCHEME

3-4 In MAGPAK, binary information is recorded serially using a self-clocking frequency-doubling scheme. A binary one is recorded as one flux reversal in a bit interval, and a binary zero is recorded as two flux reversals in a bit interval. Figure 3-1 illustrates a typical pattern.

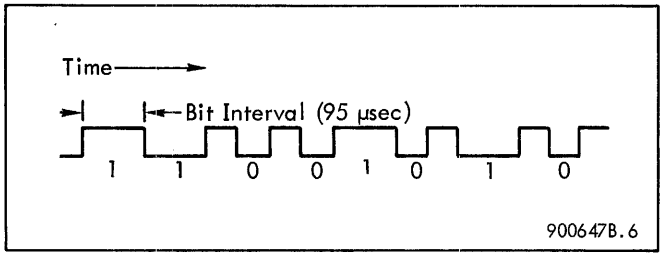

Figure 3-1. MAGPAK Coding Scheme

3-5 There is a flux reversal at the beginning of every bit interval which is used to sychronize the read decoder in playback. If a transition appears near the center of the bit interval, a zero is decoded. If no transition appears midway between synchronizing transitions, a one is decoded. Thus, all of the information is contained in the flux reversals. These reversals appear as peaks in the readback waveforms. The read electronics detect the peaks and reconstruct a square-wave signal for the read decoding logic.

3-6 At the beginning of a record, the read decoding logic must first establish synchronism with the recorded bits. A "preamable code," containing a string of logical ones, provides 8 bit times for this action to be completed.

3-7 The read decoding logic must be tolerant of variations in the playback signal which may result from speed variations, magnetic coating variations, drift in the read amplifiers, and noise. Figure 3-2 summarizes the various time intervals that the read decoding logic applies to the interpretation of the read signal.

3-8 READ DECODING TIME INTERVALS

3-9 Starting with the first transition at the beginning of each bit time, the read decoding logic generates the timing intervals indicated in figure 3-2. The most important intervals are c and e. If a read signal transition occurs in intervals c, which ranges from 31.8 μsec to 63.6 μsec after the first transition, the read decoder interprets the bit as a logical zero. If no transition occurs in interval c, the read decoder interprets the bit as a one.

3-10 Time interval e defines a period from 71.5 μsec to 127 μsec after the first transition. A read signal transition that occurs during interval e confirms synchronization for the bit under consideration and restarts all timing at zero in preparation for decoding the next bit. If no transition occurs during interval e, the read decoder times into the zone indicated in figure 3-2 as interval f. Once this happens, an overdue transition has been detected and a gap signal is generated by the read decoder.

3-11 The gap signal is interpreted by the control logic in the light of whether a postamble has occurred, and an error will be indicated if the gap appears prematurely.

3-12 Under the true gap conditions, no signals are presented to the read amplifier, and noise may supply spurious transitions to the read decoder. Interval b is the time band from 7.95 μsec to 31.8 μsec after a first transition. If a transition in the read signal appears in interval b, the read decoder interprets it as spurious and indicates gap.

3-13 There are two time intervals, a and d, which result from the fact that the read decoder derives all of its timing from a precise reference clock operating at 12 times the nominal bit rate. Interval a is called the sync quantizing interval and defines the first 7.9 μsec after the first transition. If a transition occurs within interval a, it will either be ignored or interpreted as having occurred in interval b, producing an early transition gap signal.

3-14 Time interval d as indicated in figure 3-2 is the decode quantizing interval which spans the 7.9 μsec between interval c and e. A transition that occurs during interval d can be produced only by a very marginal set of reading conditions. Even so, the read decoding logic interprets the transition conservatively. This can be shown by predicating all possible combinations of bit-pairs and clock phasing. From these circumstances only four cases are possible:

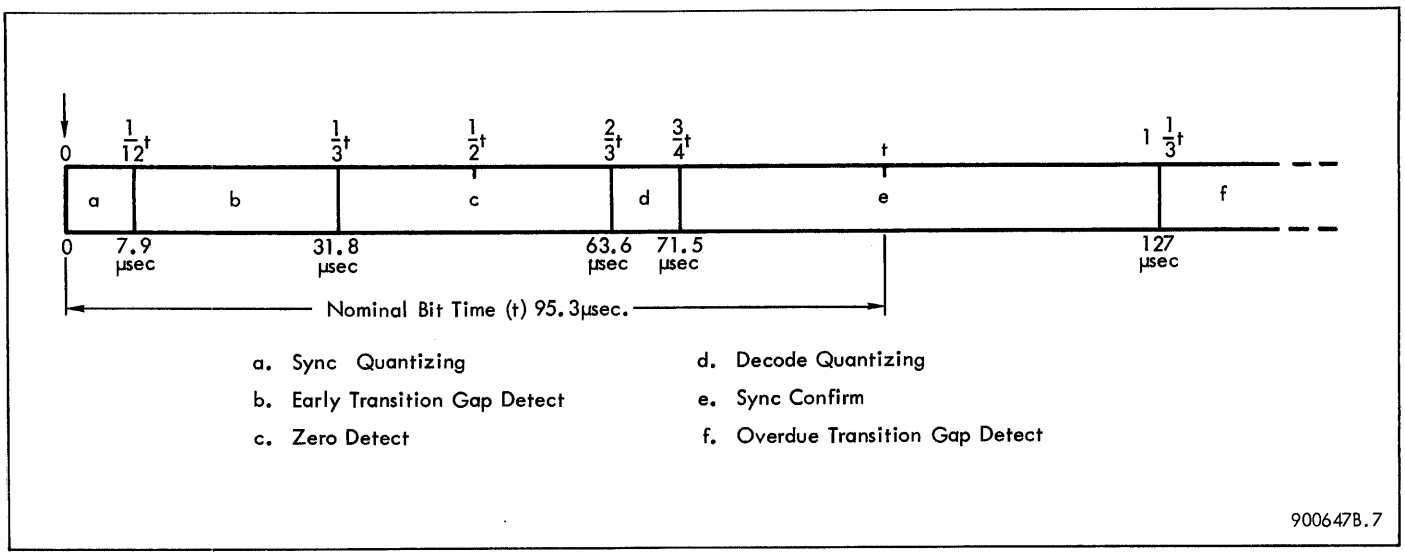

Figure 3-2. Read Decoding Time Intervals

a. The bits are read correctly, synchronism is maintained, and no error is indicated.

b. The bits are read correctly and synchronism is maintained, but an error is indicated to the computer by the gap logic.

c. The bits are read improperly and an error is indicated.

d. The read decoder is forced out of synchronism; that is, synchronism may be established on the mid-bit transitions in logical zeroes. In this case, however, the arrival of the first logical one will produce a gap error signal.

3-15 In summary, the read decoder can retrieve information correctly and maintain synchronism on signals that have been degraded by as much as -25% to +33% in time. Further degradation produces detectable errors even though the reference clock for the read decoder is running at only 12 times the nominal bit rate.

3-16 MAGPAK RECORD FORMAT

3-17 Information is recorded on MAGPAK serially in records of consecutive 7-bit characters. The number of characters per word written into a record is variable under program control. The nominal separation or gap between records is 3/4 inch. Inter-record gap is dc-erased by the writing logic.

3-18 Figure 3-3 shows the complete MAGPAK record format. The preamble code, consisting of 8 ones followed by 1 zero, is recorded just prior to the first character of each record. An odd parity bit is recorded as the first bit of each character. Immediately following the last character in the record, the postamble code is written as 1 zero followed by 8 ones.

3-19 The preamble and postamble codes are symmetrical with respect to the record so that they perform reciprocal functions as the tape is scanned in reverse. These functions may best be explained in the following summary of the reading sequence:

a. As the read head encounters the preamble, the read logic is brought into bit synchronization using the recorded ones as a reference. Only 6 of the bits are metered for validity.

b. The read logic is armed for the zero, after 7 bits are detected, the last of which must be a one. Upon receipt of the preamble zero bit, the read logic commences the character reading process.

c. The 7 bits of each character are read serially, checked for odd parity, and converted to character parallel for transmission to the computer.

d. After the last character has been read, the first 7 bits of the postamble code are detected but not transferred to the computer. The read logic is armed to confirm the validity of the postamble.

e. The read logic meters out the remaining two bits of the postamble and then detects gap normally within one bit time.

3-20 The parity test will indicate an error to the computer for all single-bit read errors and a large class of multiple-bit errors. If the read logic is out of synchronism with the record format, an error condition will very likely be detected by the parity logic.

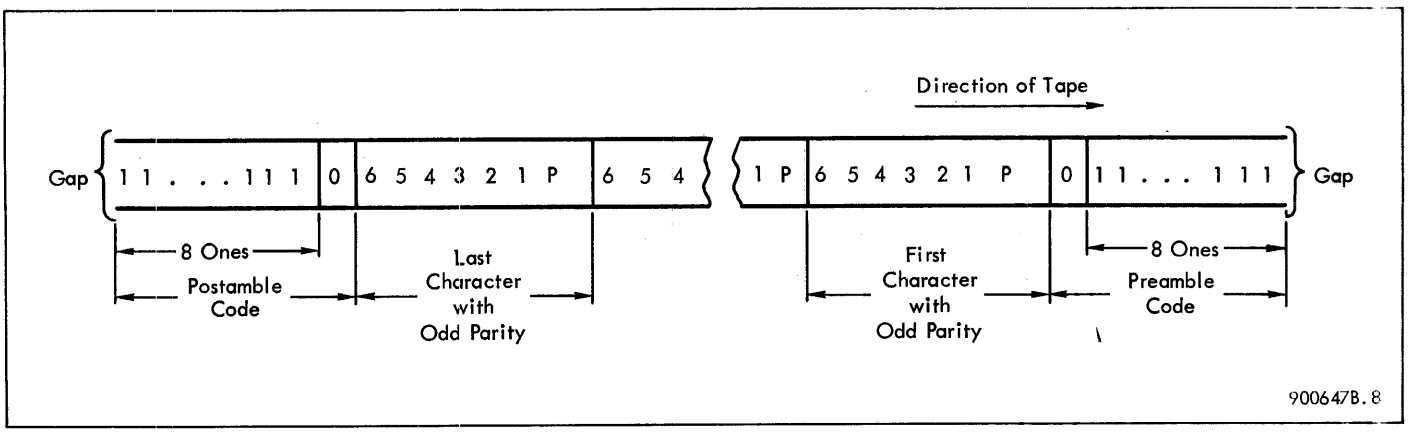

Figure 3-3. MAGPAK Record Format

3-21 It should be noted that of the 128 possible combinations of 7-bit patterns in each character position, 64 are passed as valid characters and 63 produce parity errors. One combination (0111111) does not produce a parity error directly, inasmuch as it is used to detect the postamble code. A premature appearance of this code produces an error indication by way of the gap detection logic which is described below.

3-22 The read logic indicates a gap condition whenever an absence of signal or spurious signals are read. If the gap condition is indicated before the postamble code has been detected, an error signal is transmitted to the computer and the control logic stops the tape motion.

3-23 Additionally, if a read error causes 7 bits of the postamble code (0111111) to appear prematurely as a character, the parity logic will not indicate an error as noted above. The gap condition is examined by the read logic one character time after the postamble is detected; thus if a gap condition does not exist within 4 bit times following the pattern 0111111, the premature postamble is detected as an error.

3-24 TAPE TRANSPORT UNIT ELECTROMECHANICAL DESCRIPTION

3-25 Each Model 9446 Tape Transport Unit consists of two separate tape transports mounted on a single panel, and a transport electronics assembly. The tape transports move magnetic tape over the read/write heads; the electronics assembly contains circuitry necessary to control the transports.

3-26 TAPE DRIVE SYSTEM

3-27 Forward and Reverse

3-28 Forward and reverse movement of tape is controlled by a conventional capstan-pressure roller system, consisting of a capstan motor, capstans, pressure rollers, and a drive belt. Forward and reverse movement is accomplished as follows: Signals from the computer are sent through the Tape Control Unit to the transport electronics. These signals activate a pressure roller which brings the tape into contact with one of two counter-rotating capstans, clamping the tape between the capstan and pressure roller. Tape is then driven (in the direction determined by the computer command) until the pressure roller is disengaged and the tape stops.

3-29 Capstan Motor and Pulley Hub. Capstan motor M1 is a 115-vac, 50/60-cps, single-phase, 4-pole, hysteresis synchronous motor which operates continually when relay K2 is closed. With 60-cps input, the motor rotates at 1800 rpm; at 50 cps, it rotates at 1500 rpm. As shown in figure 3-4, rotational force is transferred to the drive belt by a steel pulley hub attached to the motor shaft. A larger pulley hub is used for 50-cps operation than for 60-cps so that an identical capstan speed of 456 rpm is maintained for both frequency inputs.

3-30 Drive Belt and Idler Pulley. Force is transmitted from the capstan motor to the capstan by a 1/4-inch, flat, seamless belt which runs over the capstan motor pulley hub, pulley flywheels, and a steel idler pulley. The idler pulley, which keeps the drive belt taut, is mounted on an idler link, which, in turn, is mounted on the back-up support plate and connected to the idler spring. This spring maintains 2.7 in. lb of tension on the idler link.

3-31 Capstans and Capstan Pullies. The final step in the drive train is the transmittal of power to the capstan pullies, which are attached to the end of the capstan shafts. In addition to driving the capstans, these pullies also act as flywheels to minimize capstan speed changes. The capstan shafts rotate on two radial ball bearings. The opposite ends of the capstan shafts contain 0.31-inch-wide neoprene bands over which the magnetic tape passes.

3-32 Pressure Rollers and Solenoids. Each rubber pressure roller is mounted in a yoke and controlled by a solenoid.

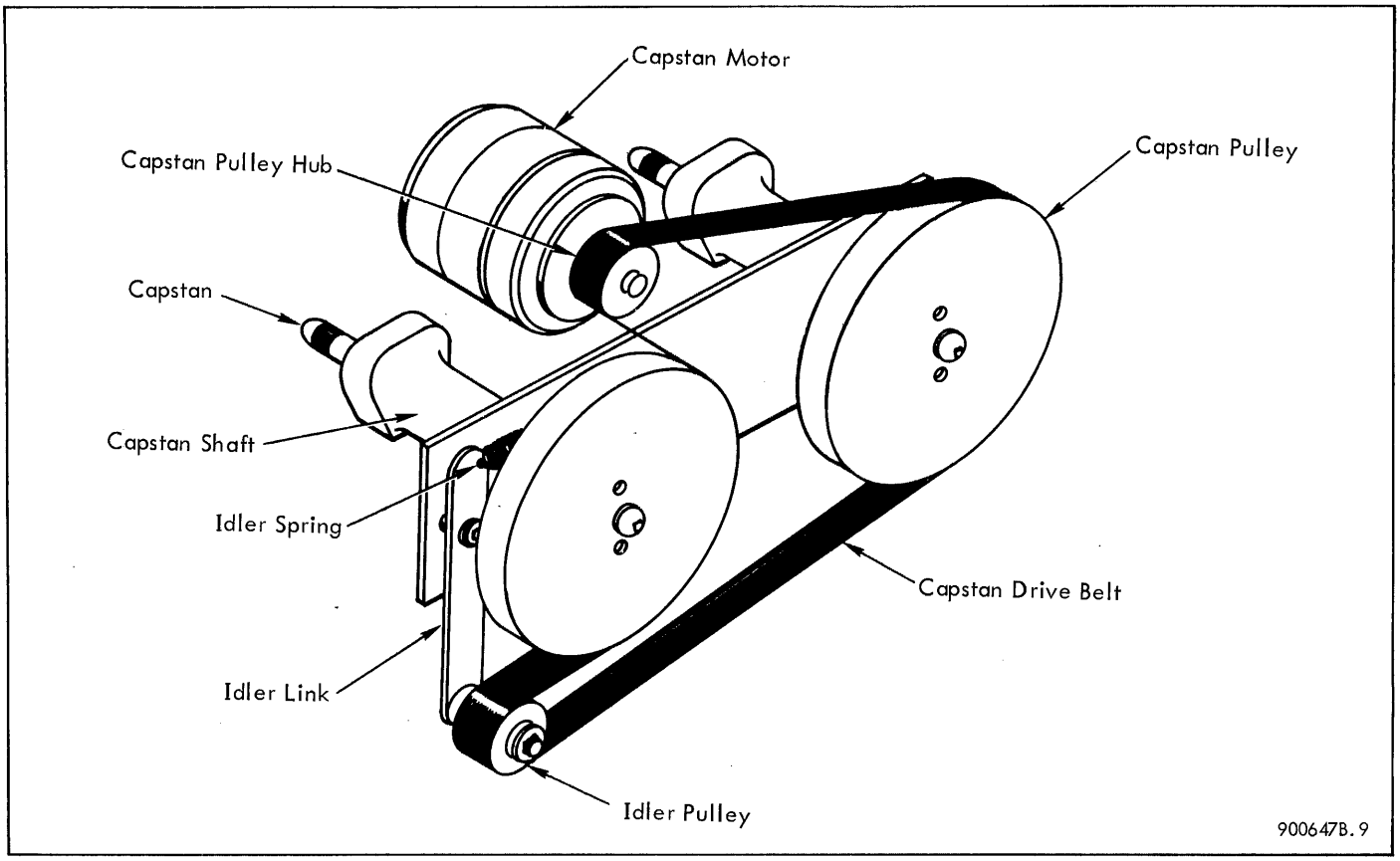

Figure 3-4. MAGPAK Tape Drive System

The pressure roller adjusting cam (eccentric) is adjusted so that a bellcrank positions the yoke with a 0.015-inch distance between the pressure roller and capstan. With relay K2 energized and K1 de-energized, +50 volts is applied to both the forward and reverse solenoids. When a FWD or REV signal is received, the respective solenoid is actuated. Upon actuation of the solenoid, the respective pressure roller closes on the capstan shaft, engages the magnetic tape (within 3 to 6 milliseconds), and accelerates the tape to acceptable data transferring speed in less than 4 milliseconds, a total maximum of 10 milliseconds after the FWD or REV signal is applied.

3-33 When the FWD or REV signal is removed from the respective solenoid, the pressure roller clears the capstan in less than 3 milliseconds. Once the pressure roller is disengaged, the tape is brought to a stop by action of the reel motor brakes and the friction in the tape path.

3-34 Reel Motor Brakes. As indicated in the equation $BRK = \overline{FWD} \cdot \overline{REV} \cdot \overline{REW}$, the reel motor brakes are applied any time tape is not in motion. With a proper armature gap of 0.003 inch, the 28-volt brakes can develop at least 20 inch-ounces of torque within 7 milliseconds after application of voltage. In actual operation, the series resistor is adjusted so that brake torque is between 3.5 and 6 inch-ounces. With this adjustment, the time constant of the brake coil and its series resistor will cause torque to build up gradually until 4 to 6 milliseconds after the stop command, ensuring that the pressure rollers are disengaged before the brakes are applied. Similarly, at the start command brake torque is removed within 3 milliseconds, ensuring that the brakes are disengaged before the pressure rollers are engaged.

3-35 Rewind

3-36 Tape is rewound by the reel motors, M2 and M3, which are 115-vac, 50/60-cps, single-phase, ac torque motors. During rewind, the torque on the left (feed) reel is increased while the torque on the right (take-up) reel is diminished such that tape rewinds in a reel-to-reel fashion without the intervention of either pressure roller. Excessive rewind speed is prevented by dynamic braking of the right reel.

3-37 Refer to figure 3-5 for the following discussion. Relay K1 closes when the REW signal is sensed. The torque on the left reel motor, M3, is increased by shorting out resistor R4 with contacts A of K1. The torque on the right reel motor, M2, is reduced by the removal of capacitor C2 from M2 when normally closed contacts B of K1 are opened. The drive of the right motor is replaced by a constant tension,

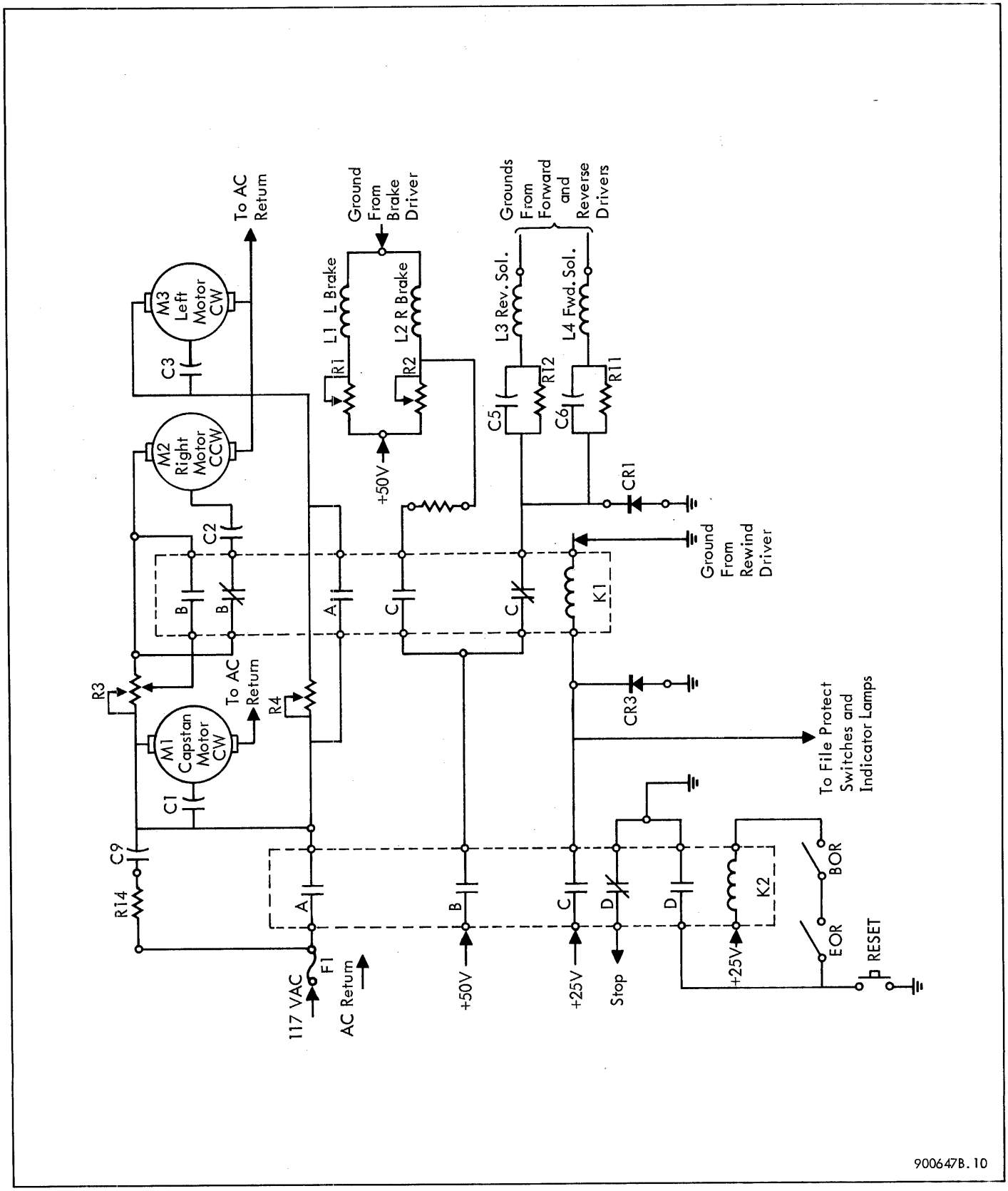

Figure 3-5. Tape Transport Unit Power Interlock Circuits

which is used to control the rewind action. This is accomplished by varying the current through M2. Resistor R3 has an adjustable tap which is switched into the current path to M2 by normally open contacts B of K1. In addition, the normally open contacts C of K1 supply a heavier current path to the right brake solenoid. This results in greater braking action on the right motor when the grounds are supplied by the brake drivers. This is necessary due to the extra speed obtained in rewinding.

3-38 TAPE SUPPLY SYSTEM

3-39 The reel motors maintain the proper amount of running tension on the tape. This results in correct tape pressure against the read/write head. Both reel motors are ac torque motors which must be adjusted for proper torque. (See section IV for adjustment procedure.) They are energized whenever power is on and relay K2 is energized; i.e., whenever a cartridge is in place and a fault condition does not exist. These motors are allowed to rotate in a "run" mode due to the release of the reel motor brakes.

3-40 When a capstan is engaged, the supply reel motor (the one whose reel is giving up tape) is driven in a direction opposite to that which it normally runs. The take-up reel motor (the one whose reel is taking up tape) rotates in its normal direction and takes up the tape as it is given up by the capstan. When the direction of tape motion changes, these motors merely interchange their roles; no switching of motor power occurs.

3-41 Several factors cause the tension of the tape to vary: diameter of tape reel, frictional drops around tension are pins and fixed guides, environmental conditions, and ac line voltage. The end result of these variable conditions is that the tension at the head can vary from approximately 2 ounces minimum to 7 ounces maximum. To accommodate this variation, reel motors with capabilities up to 5 inch-ounces stall torque are used. Additionally, nominal voltage variations are accommodated by adjustment of resistors R3 and R4.

3-42 PHOTOSENSE HEAD

3-43 A photosense assembly, shown in figures 3-6 and 3-7, is used to detect the beginning and end of tape, and to develop the BOT and EOT signals. The assembly operates

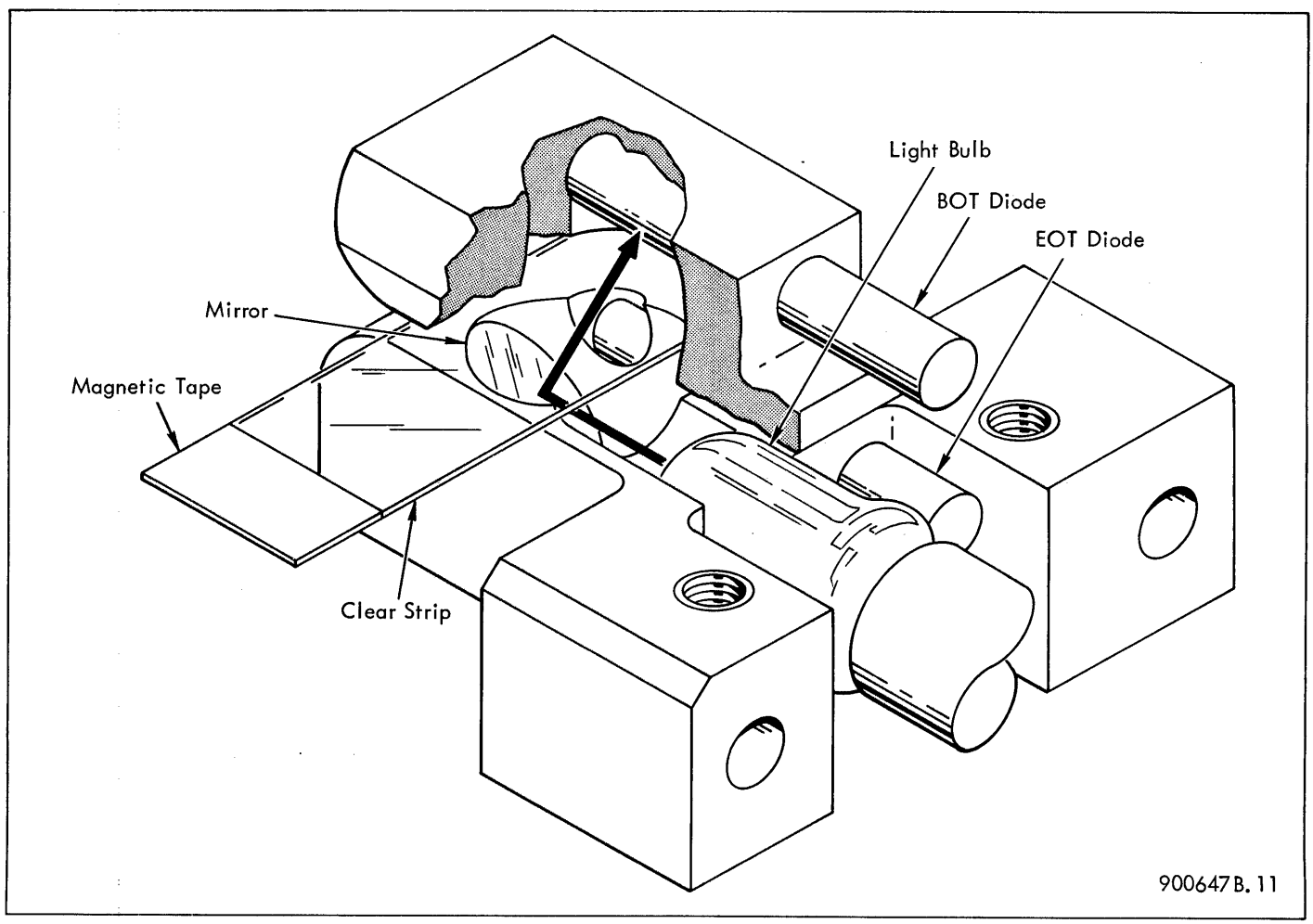

Figure 3-6. Photosense Head, Beginning-of-Tape Sensing

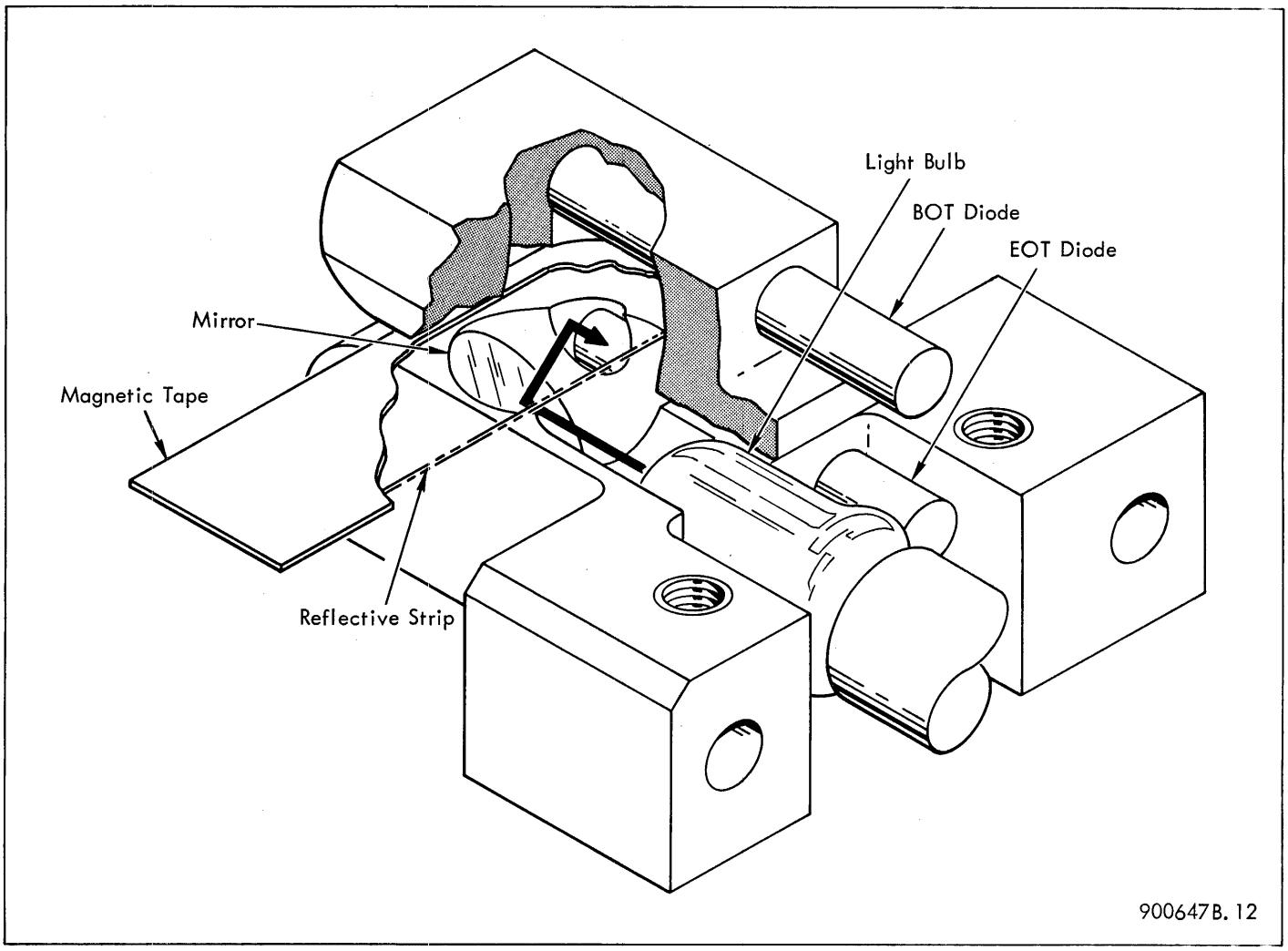

Figure 3-7. Photosense Head, End-of-Tape Sensing

by means of a light bulb (2.5-volt, 0.35-amp, TL 1-3/4, midget grooved base, C-2R filament), which provides a light source for two silicon photoconductive diodes. The photosense assembly is so constructed that light emitted from the bulb is reflected by a mirror. When the light passes through a 1.5-inch clear space of tape near the beginning of the reel, it projects on the upper photosense diode and develops the BOT signal. When the 1-inch end-of-tape reflective marker passes through the photosense assembly, light is reflected back downward and projects on the lower photosense diode, developing the EOT signal. (Note that in figure 3-7 the reflective strip is shown in phantom.)

3-44 PROTECTIVE CIRCUITS

3-45 Several circuits in MAGPAK help prevent damage to the equipment. These include a power interlock circuit, the tension arm limit switches, and the file protect switches.

3-46 Power Interlock Circuit

3-37 The power interlock circuit consists mainly of the Fault Relay, K2, and the Rewind Relay, K1. These are shown in figure 3-5. All power, except the +50 volts to the brake solenoids, is routed through the normally open contacts of K2. Therefore, in order to operate the tape transports, the Fault Relay must be energized (i.e., no fault condition present).

3-48 Once relay K2 is energized, it supplies 117 volts ac through contacts A directly to the capstan motor, M1, through R3 to the right reel motor, M2, and through R4 to the left reel motor, M3. K2 supplies +50 volts through its normally open contacts B to the normally closed contacts C of relay K1. This +50 volts is fed through RC networks to the forward and reverse pressure roller solenoids, L4 and L3. K2 also supplies +25 volts via contacts C to the file protect switches and indicator lamps. This +25 volts is also supplied to one side of the rewind relay, K1, enabling K1 to be

energized when its driver supplies a ground (during rewind only).

3-49 The energizing path for K2 is through the BOR (beginning-of-reel) and EOR (end-of-reel) contacts and the RESET button. The only way to energize K2 is by depressing the RESET button. There is then a lock-up path through the normally open contacts D of K2. Relay K2 cannot be energized if either the BOR or EOR contacts are open.

3-50 Tension Arm Limit Switches

3-51 The tension arm limit switches, S8 and S9, are spring action microswitches which are controlled by the tape tension arms and designated BOR and EOR. The following conditions cause either one or both of these switches to open:

a. Tape reaches the beginning of the reel

b. Tape reaches the end of the reel

c. A tape cartridge is being loaded (and the load handle is in the LOAD position)

d. Improper operation causes tape to bind or drag.

3-52 File Protect Switches

3-53 The file protect switches, S10 and S11, are snap-action, SPDT switches. When the contacts of these switches are in the normally closed position (i.e., when no write plug is inserted between the switch lever and the bottom of a tape cartridge), the file protect signals, FPN and FPD, are true. When the contacts are in the normally open position (with a write plug inserted), +25 volts is supplied to the write amplifiers. Thus, the file protect switches prevent accidental writing on any tape channel which should be protected.

3-54 READ CIRCUITS

3-55 The read circuits are all contained on two circuit module cards, the HX30 Gated Read Amplifier and the HX29 Data Amplifier. Refer to section V of this manual for schematic diagrams of both circuits. Figure 3-8 is a block diagram of the HX29.

3-56 HX30 Gated Read Amplifier

3-57 The HX30 contains four gated differential amplifier circuits that amplify the read head signal approximately 50 times. This stage is a so-called "long-tailed pair," an arrangement in which the emitter resistor of the differential pair is replaced by a transistor biased to present a current source to the differential emitter terminals. This provides a high degree of common mode rejection, a very desirable characteristic for amplifiers receiving signals on long leads and in a high-noise environment. The outputs of the HX30 preamplifiers are gated into the HX29 Data Amplifier.

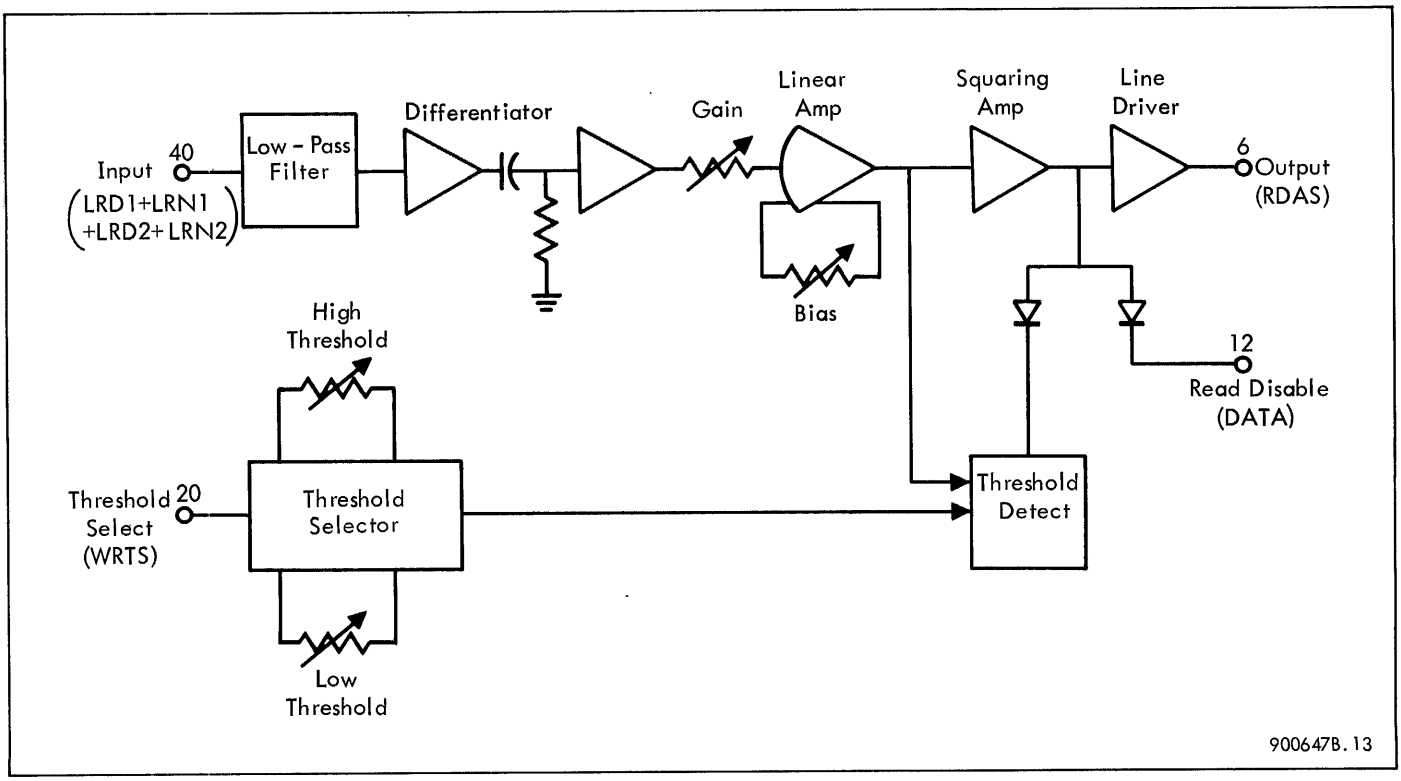

Figure 3-8. HX29 Data Amplifier Block Diagram

3-58 HX29 Data Amplifier

3-59 The HX29 contains a tape signal read amplifier which performs peak detection and has adjustable thresholds for noise rejection and amplitude check. There are two selectable thresholds, so that one level of noise rejection can be used during a read operation and another level during a read-after-write operation. The peak detection circuit is designed to operate with a frequency modulated tape signal of 4 to 12 kc. Gain is adjustable, so that the amplifier will read signals from 15 millivolts to 1.0 volt.

3-60 The HX29 can be functionally divided into seven stages: filter, differentiator, linear amplifier, squaring amplifier, line driver, threshold detector, and threshold selector. Refer to figure 3-8 for the following discussion.

3-61 Filter. The read data signals from the HX30 preamplifiers are first input to a low-pass filter, which removes line noise. The input signal frequencies are 5.5 kc and 11 kc, and the filter is designed to roll off at 25 kc. This roll-off point is as close to the uppermost signal frequency as possible without causing adverse signal attenuation.

3-62 Differentiator. The data signal output from the filter is nearly sinusoidal. The purpose of differentiating the data signal is to allow less circuitry to be used in the following stages. When the data signal is differentiated, its peaks (which correspond to flux reversals on the tape) are converted to zero crossings. It is simpler to detect and square zero crossings than an unbalanced sine wave. The output of the differentiator is a symmetrical integrated waveform whose average dc level is zero volts.

3-63 Linear Amplifier. The linear amplifier is an integrated circuit differential amplifier. A gain control is provided to accommodate a wide range of read head signal amplitudes. The linear amplifier also has a bias adjustment which can be used to balance initial dc offset and to set the output dc level. The output of the linear amplifier is fed to both the squaring amplifier and the threshold detector.

3-64 Squaring Amplifier. The squaring amplifier converts the data signal into square waves by amplifying and clipping. The circuit used is a differential amplifier with one input connected to the signal and the other input connected to the dc or quiescent level of the signal.

3-65 Line Driver. The line driver is either cut off or driven to saturation. Its input depends upon three signals:

a. The square wave data signal from the squaring amplifier

b. The read disable signal (which is enabled when the tape unit is in motion and selected)

c. The output of the threshold detector.

A false signal from any of these inputs will produce a constant true output. Since the read circuits in the tape control unit are looking for a change in the data signal, a constant true (or false) signal is interpreted as no data or gap. Provided there are no fault conditions, the driver will simply follow the data input from the squaring amplifier.

3-66 Threshold Detector. The threshold detector full wave rectifies the data signals and compares the resulting dc level against a reference threshold. This dc level is an indication of the amplitude of the read data. The threshold detector disables the line driver if it detects a low threshold level. The reference voltage can be preset to one of two levels, which are selected by the threshold select stage.

3-67 Threshold Selector. The threshold select stage selects one of two possible threshold reference voltages. Selection is controlled by a single input, WRTS. If the input is true, it selects one reference voltage; if the input is false, it selects the other. Both reference voltages can be adjusted, thereby making it possible to adjust the point at which a read or write error is detected.

3-68 TAPE TRANSPORT UNIT FUNCTIONAL DESCRIPTION

3-69 The MAGPAK Tape Transport Unit performs three main functions: status/select encoding, motion control, and data transfer. The direction of signal flow for these functions is shown in figure 3-9. Refer to this figure for the following discussion.

3-70 STATUS/SELECT

3-71 The status/select logic reports the status of a transport unit to the computer via the tape control unit. It does this in response to interrogations from the computer. The computer interrogation selects which tape unit the status is being requested upon.

3-72 MOTION CONTROL

3-73 The motion control logic stores motion commands received from the computer and transmits them to the selected tape transport. In the manual mode, pushbuttons on the transport control panel control the logic (and therefore the motion) of the tape transport.

3-74 DATA TRANSFER

3-75 The data transfer logic gates data from the selected tape transport to or from the computer. The direction of data flow depends on whether a read or write operation is in progress. Data is gated to the computer for reading and to the tape transport for writing.

3-76 TYPICAL PROGRAMMED SEQUENCE

3-77 In the AUTOMATIC mode, the computer program has complete control of tape unit operations. This is accomplished by use of magnetic tape EOM (ENERGIZE OUTPUT M) instructions. The computer monitors tape unit status

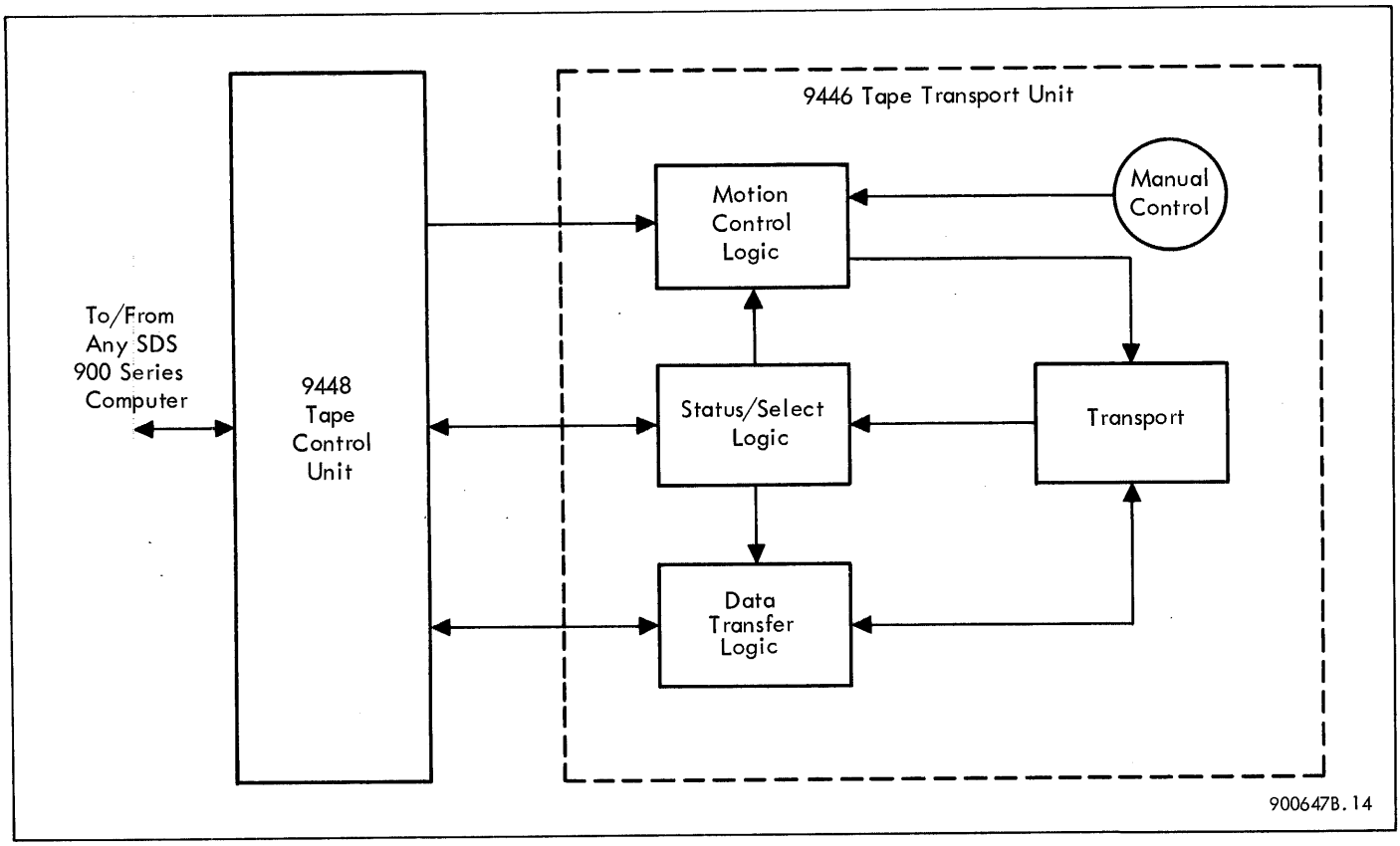

Figure 3-9. MAGPAK Functional Block Diagram

inputs for effective feedback control. A typical sequence of operations for magnetic tape is as follows: The computer alerts a buffer to select the desired tape unit; the computer then tests the status of the selected tape unit. Is it ready? Did it receive the select signal? Is it at the beginning or end of tape? Is the selected channel file protected? The computer can test any or all of these status indicators. Depending upon the results of the status tests, the computer then outputs an operation command. These operation commands, such as read, write, scan, etc., are converted to motion commands in the tape control unit. The tape transport unit then receives one of four motion commands:

a. Start Forward

b. Start Reverse

c. Rewind

d. Stop

3-78 After the motion control logic in the tape transport unit sets the mechanics of the tape unit into motion, data is channeled to or from the selected tape read or write head. This data is either presented to or taken from the tape control unit. In general, this operation continues until the computer transmits a different command. During rewind, however, if the beginning of tape is reached, a stop signal is generated by the logic in the tape unit itself.

3-79 TAPE TRANSPORT UNIT LOGIC DESCRIPTION

3-80 INTRODUCTION

3-81 A basic knowledge of the logic used in SDS computers is essential to the understanding of logical functions performed by MAGPAK. For purposes of discussion and brevity, many logic equations in the following paragraphs show only part of their gate mechanizations. A complete listing of tape transport unit logic equations and a glossary of logic terms are included at the end of this section. Logic diagrams, showing connector and pin locations of signals, are included in section V of this manual.

3-82 Figure 3-10 is a simplified logic diagram showing the three main logical functions of the tape transport unit: status/select, motion control, and data transfer. It also shows the interface between the tape control unit, the tape transport unit electronics, and the transport/control panel assembly. The tape unit shown in figure 3-10 is transport No. 1; the logic for transport No. 2 is the same except that signals are labeled differently. For example, TSA1 refers to station No. 1, and TSA2 refers to station No. 2. Certain circuits such as the read amplifier and the CHSB flip-flop, however, are common to both transport units.

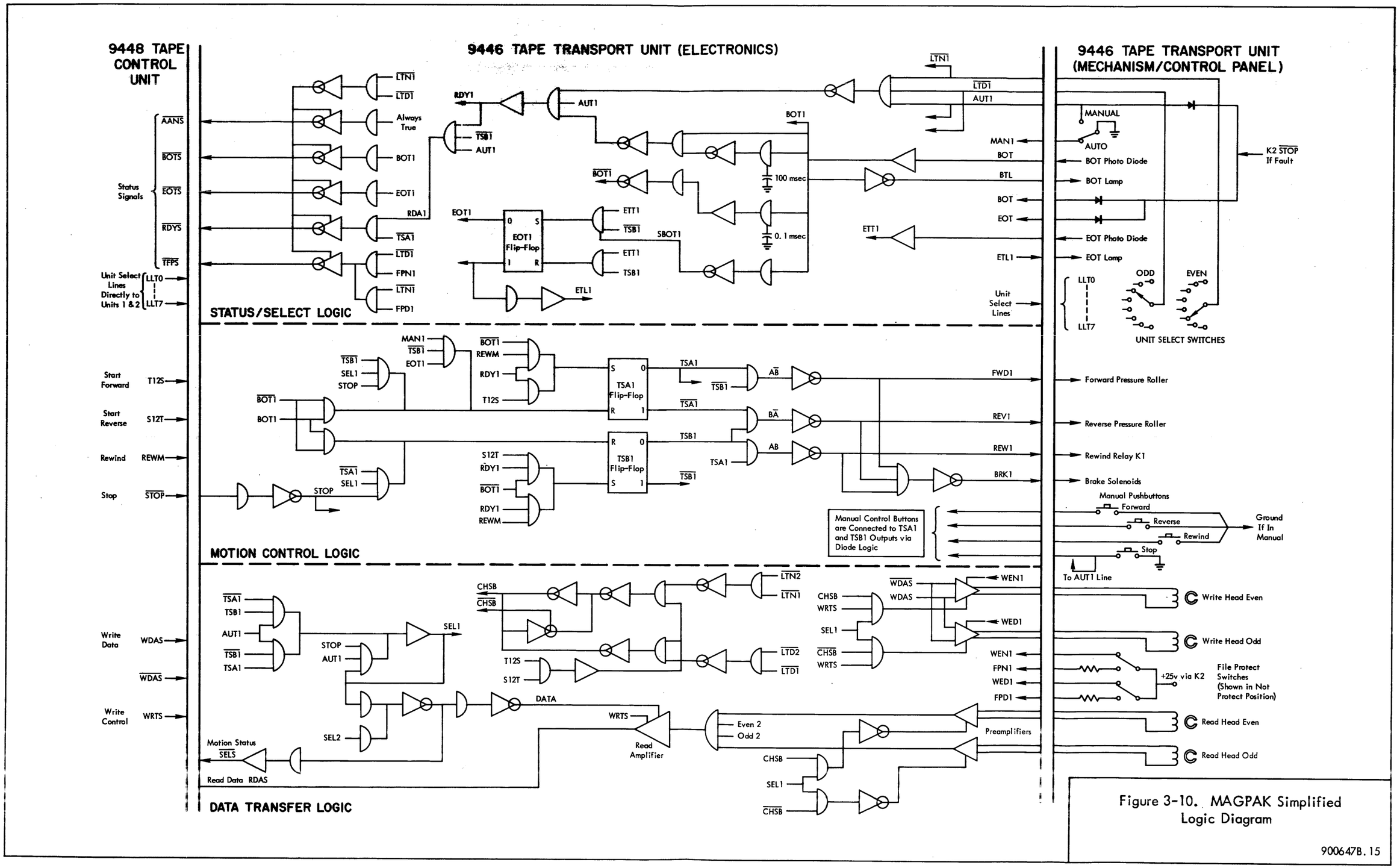

Figure 3-10. MAGPAK Simplified Logic Diagram

900647B.15

3-83 STATUS/SELECT LOGIC

3-84 Unit Select Lines

3-85 Operation of a tape station is initiated when the proper address is selected on the incoming unit select lines (LLT0 to LLT7). These lines are routed through Cable Plug Module P84 to all tape stations in the system. The unit select lines are connected to the UNIT SELECT switches on the transport control panel. An active unit select line will be grounded. The active line is determined by the setting of the UNIT SELECT switch. The ground is sent back to the status/select logic as either $\overline{LTD1}$ or $\overline{LTN1}$ (for tape station No. 1). $\overline{LTD1}$ refers to the odd channel and $\overline{LTN1}$ to the even channel.

3-86 The first status signal that must be sent back to the tape control unit is the select acknowledge ($\overline{AANS}$) signal. This signal is at ground when it represents an acknowledge condition.

$$\overline{AANS} = \overline{LTD1} + \overline{LTN1} + \overline{LTD2} + \overline{LTN2}$$

The above equation is derived in the following manner. $\overline{LTN1}$ and $\overline{LTD1}$ are AND'ed together and input to an inverter. Therefore, if either $\overline{LTN1}$ or $\overline{LTD1}$ are at ground (indicating that the odd or even channel of tape station No. 1 has been selected), the output of this inverter will be true. This true output enables the common input of all the status inverters. Since the inverter used to develop $\overline{AANS}$ has a constant true input, the output will be pulled to ground when its common input swings true. An identical inverter for tape station No. 2 is OR'ed into the $\overline{AANS}$ line. This inverter will produce a ground if either $\overline{LTN2}$ or $\overline{LTD2}$ is selected.

3-87 Ready

3-88 The tape station is ready provided it is in the automatic mode, no motion is in process, and no fault condition exists. A fault condition occurs when tape comes to the physical end or beginning, or a cartridge is unloaded. When the fault condition is cleared and the RESET pushbutton is depressed, the AUTO signal goes true and the unit is again ready.

$$RDY = (\overline{LTN} + \overline{LTD})\ AUT\ \overline{FWD}\ \overline{REV}\ \overline{REW}$$

where:

$$AUT = K2D\ AUTO\ SWITCH$$

$$sK2 = \overline{BOR}\ \overline{EOR}\ RESET\ BUTTON$$

$$\overline{FWD}\ \overline{REV}\ \overline{REW} = \overline{TSA}\ \overline{TSB}$$

3-89 Logic is also provided to assure that if the beginning-of-tape point is being approached, the ready signal will be inhibited until tape motion has stopped. This is necessary to ensure that the load point is always started close to the same point. The logic consists of the beginning-of-tape signal, BOT, and a delayed beginning-of-tape signal, BTS, AND'ed together to drive an inverter. This inverter will inhibit the development of the ready signal when its output is false.

3-90 When a tape unit is not at the beginning-of-tape point, a capacitor on Cable Plug Module P84 discharges to ground and supplies a false input to an inverter; this, in turn, arms one leg of an AND gate. The other leg of this AND gate is at ground because the BOT signal is false. This makes the output of an inverter fed by this AND gate true. Therefore, the ready signal is not inhibited at that time.

3-91 When a tape unit reaches the beginning-of-tape point, the BOT signal goes true and the capacitor on P84 starts to charge. For the duration of the charge time, the inverter it drives is still held true. During this time, the AND gate has both inputs true and thus the inverter it drives is held false. This inhibits the ready signal until the capacitor charges to a level sufficient to switch the inverter it drives. The time required to charge the capacitor to this level is approximately 100 milliseconds, which is ample time for tape motion to come to a stop.

3-92 End-of-Tape

3-93 End-of-tape status is indicated by the end-of-tape flip-flop being set. This occurs when the tape unit has been going in a forward direction and the end-of-tape reflective marker has been encountered. The end-of-tape flip-flop is reset when tape is moving in the reverse direction and the end-of-tape marker is sensed. The end-of-tape flip-flop is also reset any time there is a fault condition.

$$sEOT = (ETT1\ \overline{TSB1})\ SBOT1$$

$$rEQT = \overline{K2} + ETT1\ TSB1 + - - -$$

where:

$$ETT1 = EOT$$

$$\overline{TSB1} = FWD1$$

$$TSB1 = REV1 + REW1$$

$$SBOT1 = BOT$$

3-94 Beginning-of-Tape

3-95 The beginning-of-tape signal (BOT) is present when the tape station is positioned such that the beginning-of-tape clear space is stationed at the photosense head. As shown in figure 3-10, $\overline{BOT1}$ is generated in the same manner as the ready inhibit circuitry. $\overline{BOT1}$ is used in a reset function of the motion control logic. When BOT is approached, the true pulse caused by the delay of $\overline{BOT1}$ will reset the TSA and TSB flip-flops.

3-96 File Protect

3-97 The file protect signal is true if there is no write plug inserted for the channel that is being tested. For example, if the write plug is missing on the odd channel of one of the tape stations, and that channel is interrogated for file protect, the response will be file protected. A similar response is involved when checking for the even channel.

$$\overline{TFPS} = FPN1\ \overline{LTD1} + FPD1\ \overline{LTN1} + FPN2\ \overline{LTD2} + FPD2\ \overline{LTN2}$$

In the above equation, signals FPD1 and FPN1 are true when the file protect switches are closed for the odd and even channels (respectively) of tape station No. 1. Similarly, FPD2 and FPN2 are true when the odd or even channels of tape station No. 2 are file protected. $\overline{LTD1}$, $\overline{LTN1}$, $\overline{LTD2}$, and $\overline{LTN2}$ are generated when the odd or even tracks of either tape station have been selected.

3-98 If both the file protect switches for a particular transport are in the non-protect position, the output of the $\overline{TFPS}$ inverter is true. This is because both input AND gates are disabled by false inputs on FPD and FPN. As in all status lines, both transports have identical logic OR'ed into one line.

3-99 The file protect switches also create write enable signals, WED1, WEN1, WED2, and WEN2. These signals are used to enable the write amplifiers for their respective tape channels. For example, WEN1 will supply an enabling voltage to the write amplifier for the even track of tape station No. 1 when the file protect switch for that track is not in the protect position.

3-100 Indicators

3-101 The indicator lamps on the tape transport unit control panel are turned on by the following signals:

LOAD POINT (BRL)	= BOT
READY (RDL)	= RDY
END OF TAPE (ETL)	= EOT
FILE PROTECT ODD	= FPD
FILE PROTECT EVEN	= FPN

These indicators are driven by an IK51 Inverter Amplifier. When a transport unit is in operation and the indicator is OFF, a small current is present in the indicator. This reduces the initial start current of the bulb to a level that can be handled by the driver. The bulbs are always prewarmed before use since all bulbs are in the OFF state during a power-on sequence.

3-102 MOTION CONTROL LOGIC

3-103 The basic motion of the tape transport unit is controlled by the TSA and TSB flip-flops. When both flip-flops are reset, the transport is stopped. When TSA is set, the transport is going forward; with TSB set, the transport runs in reverse. With both TSA and TSB set, the unit is rewinding.

$$\text{No Motion} = \overline{TSA}\ \overline{TSB}$$

$$\text{FWD} = TSA\ \overline{TSB}$$

$$\text{REV} = \overline{TSA}\ TSB$$

$$\text{REW} = TSA\ TSB$$

3-104 The TSA and TSB flip-flops are set and reset by signals from either the tape control unit or pushbuttons on the transport control panel in conjunction with status signals (i.e., beginning-of-tape, end-of-tape, ready, etc.) from the transport. All operations are completely interlocked so that no sequencing of any control panel buttons or commands from the tape control unit will cause tape damage. The fault relay, K2, prevents erroneous tape operation during a power-on sequence. Also, K2 disconnects power from the unit if a fault occurs while the transport is operating; no further operations are possible until the operator intervenes.

3-105 Manual Control

3-106 The tape station can be run from the control panel with the AUTO-MANUAL switch in the MANUAL position, providing a tape cartridge is in place and the RESET pushbutton has been pressed. In order for the tape station to reset, the end-of-reel and beginning-of-reel switches must be closed.

$$sK2 = \overline{BOR}\ \overline{EOR}\ \text{RESET Button}$$

If the beginning-of-reel or end-of-reel switches open after operation has commenced, the transport will become disabled after approximately 100 milliseconds.

$$rK2 = BOR + EOR$$

The time delay is inserted to prevent spurious signals from causing a fault condition (e.g., a tape tension arm momentarily opening the BOR or EOR switch).

3-107 In the manual mode of operation, the tape station will not respond to any commands from the tape control unit. This is because the set input gates of the TSA and TSB flip-flops are inhibited by the ready signal. RDY is held false by AUT, which is at ground when the unit is in the manual mode. The control panel pushbuttons directly set or reset the appropriate flip-flops by directly grounding the true or false outputs.

3-108 A diode network located on Cable Plug Module P82 is used to select the true or false side of the TSA and TSB flip-flops. These diodes decode which flip-flops are to be set or reset from each control panel button. For example, if the FORWARD button is pushed, a ground is applied to the false output of TSA and the true output of TSB. TSA is

then forced to set and TSB to reset. This is decoded to produce an enable signal to the forward pressure roller. The decoding logic for the three motion functions can be expressed:

$$FWD1 = TSA1\ \overline{TSB1}$$

$$REV1 = \overline{TSA1}\ TSB1$$

$$REW1 = TSA1\ TSB1$$

The brake solenoids are activated if none of the above equations are satisfied:

$$BRK1 = \overline{FWD1}\ \overline{REV1}\ \overline{REW1}$$

This decoding logic is used in both manual and automatic modes.

3-109 The reset function of $\overline{BOT}$ is also common to both modes. $\overline{BOT}$ will reset both motion flip-flops when the beginning-of-tape (load point) is approached:

$$rTSA1 = \overline{BOT1}\ BOT1 + - - -$$

$$rTSB1 = \overline{BOT1}\ BOT1 + - - -$$

BOT1 is true when beginning-of-tape is sensed; $\overline{BOT1}$ is true when the unit is not at the beginning-of-tape and when BOT1 has just been sensed. This logic stops the transport at load point no matter what motion is in progress. In manual, any motion can be reinitiated from load point.

3-110 If the transport is in manual and moving forward, it will stop when the end-of-tape marker is encountered:

$$rTSA1 = MAN1\ (\overline{TSB1}\ EOT1 + - - -) + - - -$$

In this equation, TSB1 is reset for forward motion and EOT1 is the end-of-tape signal. After the end-of-tape marker is sensed in the forward direction, only reverse or rewind operation is possible because TSA is held reset by EOT1.

3-111 Automatic Control

3-112 The basic operation of forward and reverse motion in automatic is the same as in manual; the only difference is in the method of setting and resetting the particular flip-flops. In order for either TSA or TSB to be set, the tape station must be in the automatic mode, addressed, and there must be no rewind stop delay in process:

$$sTSA1 = RDY1\ (\overline{BOT1}\ REWM + T12S) + - - -$$

$$sTSB1 = \overline{BOT1}\ RDY1\ (REWM + S12T) + - - -$$

where:

RDY1 = AUT (LTN1 + LTD1)
$\overline{BOT1}$ = Not in load point delay time
S12T = Start reverse
T12S = Start forward
REWM = Rewind

3-113 There are four commands from the tape control unit that are recognized by the tape station when it is addressed and in automatic. These commands are: start forward (T12S), start reverse (S12T), stop (STOP), and rewind (REWM). Forward, reverse, and rewind are the only commands that will set the motion flip-flops. The start forward command sets TSA; the start reverse command sets TSB. Rewind sets both TSA and TSB, and stop resets both TSA and TSB. The tape station will ignore rewind and reverse commands if it is at load point. $\overline{BOT1}$ disables all input set gates except the forward gate:

$$sTSA1 = RDY1\ T12S + - - -$$

3-114 Both forward and reverse motions can be stopped at any time:

$$rTSA1 = \overline{TSB1}\ SEL1\ STOP\ (\text{stop forward}) + - - -$$

$$rTSB1 = \overline{TSA1}\ SEL1\ STOP\ (\text{stop reverse}) + - - -$$

where:

$$SEL1 = AUT1\ (\overline{TSA1}\ TSB1 + TSA1\ \overline{TSB1}) + - - -$$

A rewind operation, however, can not be stopped with the stop command. This is because in rewind both flip-flops are set; in order for either flip-flop to reset, the opposite flip-flop must already be in a reset condition.

3-115 DATA TRANSFER LOGIC

3-116 Data can be read or written on either the odd or even channel of any tape station. Selection of the odd or even channel for a particular tape station is accomplished at the time of command. If the even channel has been selected, the CHSB flip-flop will be set:

$$sCHSB = (\overline{LTN1} + \overline{LTN2})\ (T12S + S12T)$$

Selection of an odd channel resets CHSB:

$$rCHSB = (\overline{LTD1} + \overline{LTD2})\ (T12S + S12T)$$

3-117 Selection takes place when the tape unit is in automatic and any motion is in process except rewinding:

$$SEL1 = AUT1\ (TSA1\ \overline{TSB1} + \overline{TSA1}\ TSB1) + - - -$$

The select line ($\overline{SELS}$) goes active back to the control unit to indicate that data is, or should be, transferred to or from a transport unit. Once a unit is selected, de-selection does not take place until after the stop pulse goes false (approximately 10 msec after STOP goes true):

$$SEL1 = STOP\ AUT1\ SEL1 + - - -$$

3-118 Reading

3-119 A preamplifier/postamplifier system is used to retrieve the digital data written. (The theory of operation of these

circuits is covered under "Read Circuits.") There are four preamplifiers on one HX30 Gated Read Amplifier circuit module. Each tape read head feeds one of these preamplifiers. The particular preamplifier to be activated is selected by the select signals and the output of the channel select flip-flop:

$$SEL1\ CHSB + SEL1\ \overline{CHSB} + SEL2\ CHSB + SEL2\ \overline{CHSB}$$

The select signals also activate the postamplifier:

$$DATA = SEL1 + SEL2$$

These select signals allow the read amplifier to operate only when the transport is in motion:

$$SEL1 = AUT1\ (TSA1\ \overline{TSB1} + \overline{TSA1}\ TSB1) + - - -$$

The outputs of the HX30 preamplifiers are OR'ed into the input of the HX29 postamplifier.

3-120 A write select signal (WRTS) from the tape control unit is used in the postamplifier to select the threshold. During normal read operations, WRTS is false, causing a low threshold in the amplifier. During write operations, a read-after-write check is performed. WRTS is then true and a high threshold is selected. This makes the read-after-write check more sensitive to the detection of write errors.

3-121 Writing

3-122 Write selection is similar to read selection, but is further qualified. First, there must be a write plug in the tape cartridge corresponding to the channel to be written. Second, the write select line (WRTS) must be active from the tape control unit. For example, writing on the odd channel of tape station No. 1 is selected by:

$$SEL1\ \overline{CHSB}\ WRTS\ WED1$$

In this expression WED1 supplies collector voltage to the odd channel write amplifier provided the file protect odd switch is closed. WEN1 performs the same function for the even channel write amplifier. Write selection also activates the associated read selection, thus allowing a read-after-write check at the tape control unit.

3-123 Writing is controlled by the tape control unit. Information is written on the tape in a saturation mode. The data that is placed on the tape is dependent upon the two write lines (WDAS and $\overline{WDAS}$) from the tape control unit.

3-124 TAPE CONTROL UNIT FUNCTIONAL DESCRIPTION

3-125 The 9448 MAGPAK Tape Control Unit can be divided into four functional sections as indicated in figure 3-11. The heavy lines in figure 3-11 distinguish information flow from control signal paths. The control logic section interprets EOM commands and addresses. This section coordinates the tape motion command sequences with the information transfers into and out of the computer. The Harvey register section has as its primary functions the conversion of parallel computer output signals to serial for writing and serial playback signals to character parallel in reading. The Harvey register also operates in a counting mode to provide timing signals to the control logic. The write logic section encodes the serial signals into frequency-doubling bit format. The dc erase signals are also generated in the write logic. The read logic section decodes the frequency-doubling bit format, maintains bit synchronism on the playback signal, and detects gap. Additionally, the read logic detects the preamble, checks character parity on the playback information, and signals the end of a record as the postamble is detected.

3-126 WRITE LOGIC SECTION

3-127 Figure 3-12 shows the write logic section separated into functional groupings of flip-flops. The reference clock, FC, is the precision source of timing pulses for writing. The FC signal runs at 12 times the bit transfer rate or 126 kc. This signal is used throughout the MAGPAK Tape Control Unit as a flip-flop clocking term.

3-128 Write Clock Generator

3-129 Under the control of gates generated in the control logic section, the write clock generator flip-flops (WCA-WCD) divide the reference clock frequency by 12, producing two symmetrically out-of-phase write clocks, WCP0 and WCP1. Information shifting in the Harvey register is strobed into the write flip-flop, WF, by WCP0 causing the write signal, WDAS, to make a transition for each logical zero. The WCP1 pulse always toggles WF to its opposite state, producing the synchronizing transition in each recorded bit.

3-130 Write Synchronizer

3-131 The write synchronizer (WSA-WSC) counts the WCP0 pulses. Every seventh pulse, the write character gate, WGO1, is generated. The control logic uses the WGO1 gate to initiate the output of a character from the computer during writing operations.

3-132 The write logic section is enabled by the control logic whenever the computer buffer is addressing MAGPAK. Thus, the WGO1 pulses are available for timing certain MAGPAK operations. These pulses, which occur at a 1.5-kc rate, are counted in the Harvey register to provide delays and intervals in the starting and stopping sequences. Also, the control logic uses WGO1 as a standard time for state changes.

3-133 READ LOGIC SECTION

3-134 Figure 3-13 shows the read logic section separated into functional groupings of flip-flops. The reference clock, FC, is the same precision source of timing pulses that is used for writing.

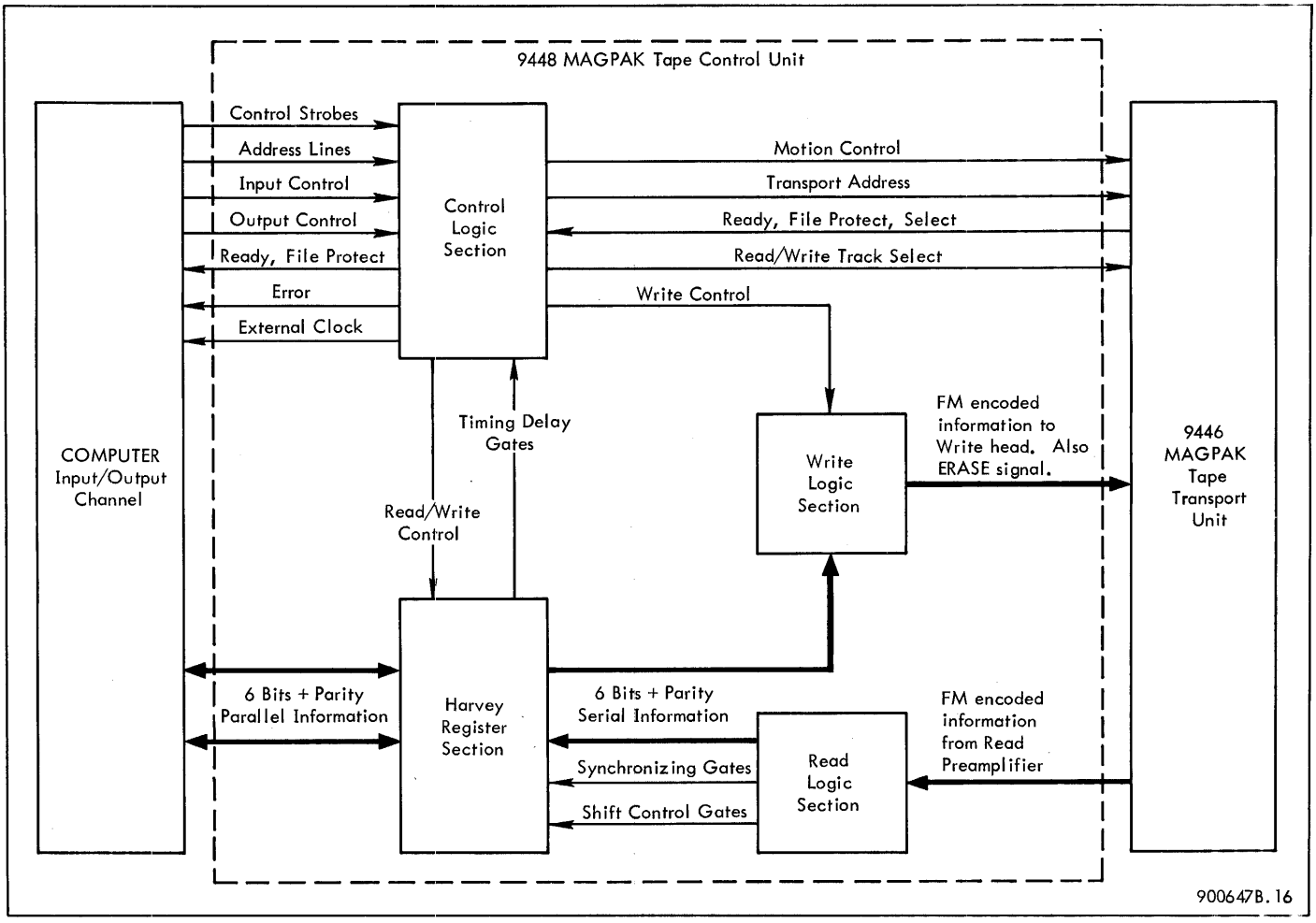

Figure 3-11. Tape Control Unit Block Diagram

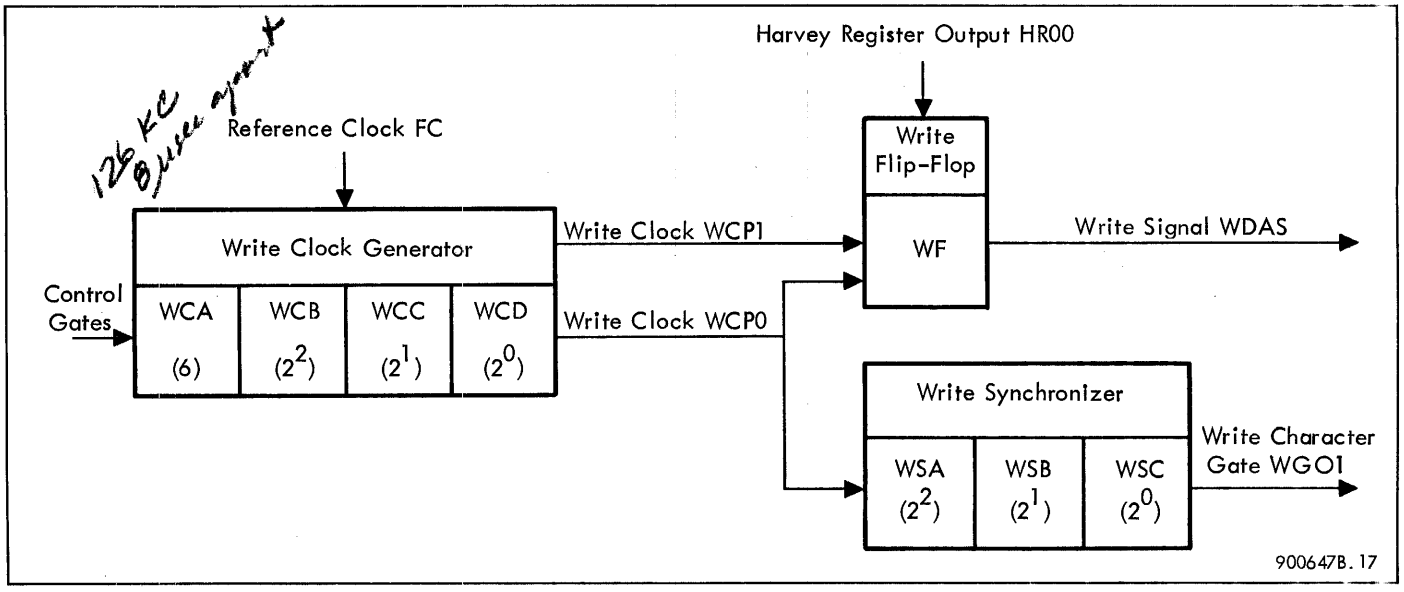

Figure 3-12. Write Logic Section Block Diagram

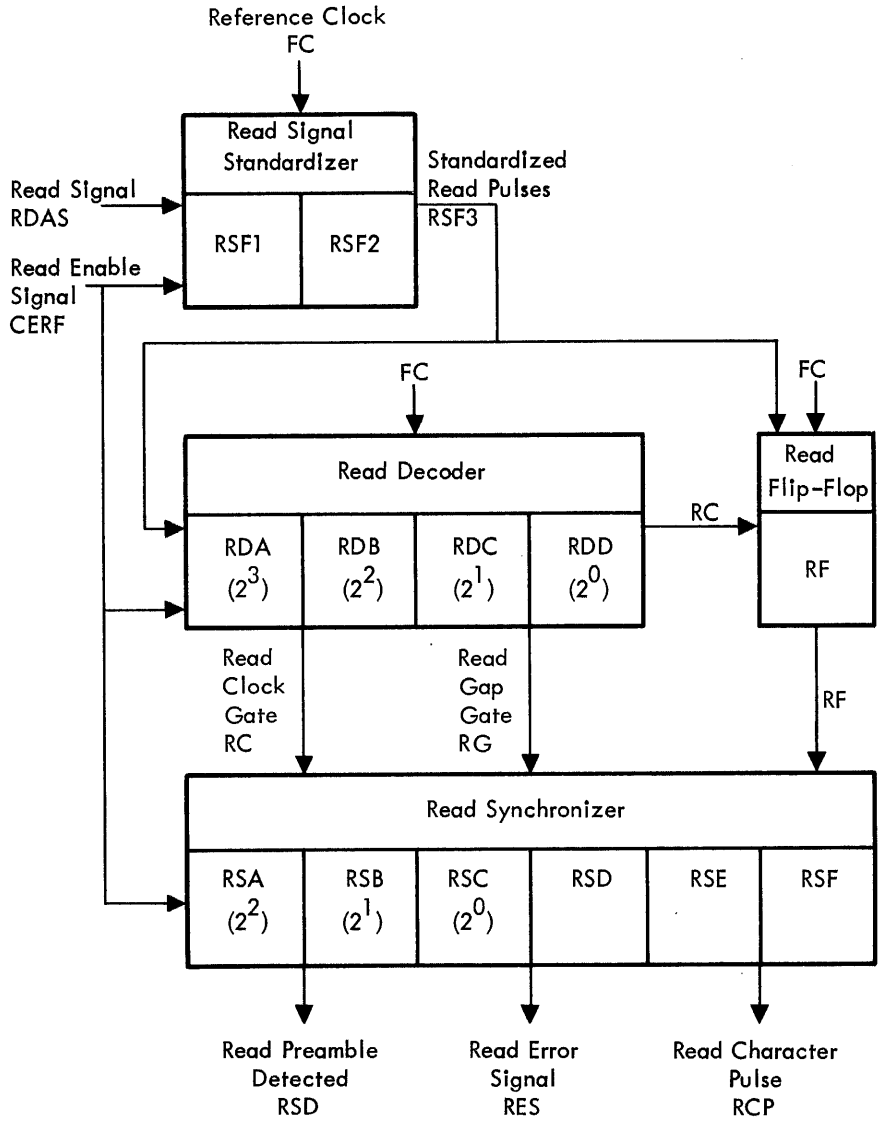

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Figure 3-13. Read Logic Section Block Diagram

3-135 Read Signal Standardizer

3-136 In the read signal standardizer, FC is used to clock the read signal, RDAS, into RSF1 and then into RSF2. The outputs of these flip-flops are delayed versions of the RDAS square wave. By gating RSF1 with RSF2, a set of read pulses, RSF3, are generated which provide a quantized representation of the zero-crossings in the RDAS.

3-137 Read Decoder

3-138 The read decoder, RDA-RDD, operates as a variable period binary counter clocked by FC and synchronized by RSF3 pulses. The counter is uncaged by an RSF3 pulse and starts counting upward from zero. The contents of the counter define the time intervals shown in figure 3-2. A gap condition will be recognized in the read decoder which stalls and waits for another zero-crossing. As preamble ones arrive, the counter receives only synchronizing transitions on RSF3 for 8 bit times.

3-139 Thus, the counter receives RSF3 pulses during the sync confirm time interval only. If a transition occurs within the zero detect time interval, the read decoder indicates the arrival of a zero but does not reset. Once the read decoder establishes synchronism, only the RSF3 pulses that arrive within the sync confirm time interval will reset the counter.

3-140 As the read decoder cycles, the read clock, RC, is generated for each bit time. The read gap signal, RG, is supplied whenever a spurious transition is detected during the first third of a bit time, or when no transition is detected until after the read decoder has counted to a state representing 1-1/3t bit time.

3-141 Read Flip-Flop

3-142 The read flip-flop, RF, is used to convert the frequency-modulated signal to binary. This conversion is accomplished by arming RF at each read clock, RC, and resetting RF to zero on any RSF3 that occurs within the zero decode time interval as defined by the read decoder. The content of RF is strobed by RC in subsequent logic.

3-143 Read Synchronizer

3-144 The Read Synchronizer, RSA-RSF, performs six functions:

a. The preamble code is detected. The arrival of the preamble zero establishes the read synchronozer in synchronism with the characters of the record.

b. Character synchronism is maintained within the read synchronizer by counting in 7-bit cycles through the record.

c. Serial odd-parity errors are detected.

d. If a read gap signal, RG, occurs during character processing, the read synchronizer indicates an error.

e. The first seven bits of the postable are detected and character processing is terminated.

f. The postable is confirmed when the read synchronizer is reset by a read gap signal, RG, prior to the arrival of another character.

3-145 The read synchronizer is clocked by the read clock, RC, and performs its functions by interpreting the read flip-flop, RF, and read gap, RG. Once it is enabled by the control logic, the read synchronizer functions autonomously during write as well as read operations.

3-146 It is desirable to consider the read synchronizer flip-flops to be divided according to function as follows: RSA-RSC act as a seven-state binary counter; RSD detects the preamble; RSE is the parity error detect flip-flop; and RSF detects the postable.

3-147 The primary outputs of the read synchronizer are the read character pulse, RCP, which indicates the arrival of the seventh bit in each character, the read error signal, RES, and the read preamble detect, RSD.

3-148 HARVEY REGISTER SECTION

3-149 Figure 3-14 shows the Harvey register flip-flops, HR00-HR06. This general-purpose register performs four functions:

a. Acting as a shift register, the Harvey register converts the character parallel signals from the computer buffer into serial for recording. Likewise, during reading, the serial information is converted to character parallel for inputting to the computer buffer. In order to accommodate reverse scan, the Harvey register is capable of reverse shifting.

b. The indicated parallel transfers described above are mechanized in the Harvey register section.

c. During reading or scanning, the file mark is detected within the Harvey register. Additionally, in order to maintain program compatibility with conventional magnetic tape, it is necessary to record file marks as two characters even though the computer outputs only one. This function is performed in the Harvey register.

d. The timing of all starting, stopping, and continue sequence is performed by the Harvey register. Inasmuch as no information-transfers take place when this function is required, the Harvey register is converted to a binary counter from which seven time intervals are decoded.

3-150 The read flip-flop signal, RF, is supplied to the Harvey register along with the read clock, RC, during reading and scanning operations. For read and scan forward, bits from RF shift into HR06 and then through the register, clocked by RC to HR00. The computer buffer is clocked by the control logic at the read character pulse (RCP) time,

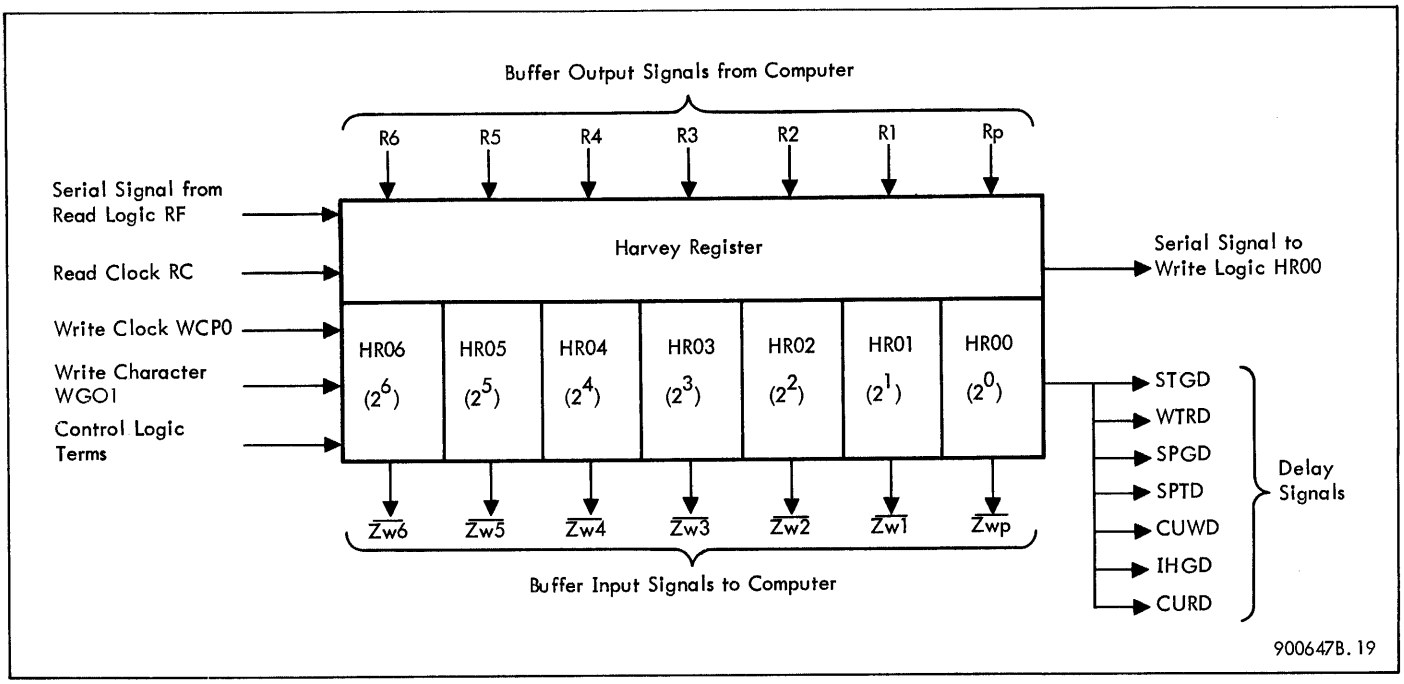


Figure 3-14. Harvey Register Block Diagram

after which the HR00-HR06 contents are transferred in parallel. For scan reverse, the sequence is the same except the bits shift from RF into HR00 first, and then backwards through the register to HR06.

3-151 During writing, the computer buffer is clocked by the control logic at the write character WGO1 time after which the HR00-HR06 are loaded in parallel. Under the control of the write clock, WCP0, the Harvey register shifts forward from HR06 to HR00. The output of HR00 is the serialized character processed by the write flip-flop, WF. Since it may be necessary to repeat the character to duplicate the dual file mark, the Harvey register is arranged to recirculate its contents during shifting. If the output is only one character, therefore, it is recorded twice on the tape. This action is defeated if the output is more than one character in any record.

3-152 The Harvey register is used as a binary counter under conditions defined by the control logic. The write character pulses, WGO1, are used as a precise 1.5-kc clock for this function. The time intervals defined by recognition of Harvey register states may be summarized as follows:

STGD	StarT Gap Delay	(36.0 ms)
WTRD	Write To Read Delay	(34.7 ms)
SPGD	StoP Gap Delay	(26.0 ms)
SPTD	StoP Tape Delay	(30.7 ms)
CUWD	ContinUe Write Delay	(60.7 ms)
CURD	ContinUe Read Delay	(75.5 ms)
IHGD	InterHead Guard Delay	(50.7 ms)

3-153 CONTROL LOGIC SECTION

3-154 Figure 3-15 shows the control logic section partitioned according to functional groups of flip-flops and gating. In addition to the control elements listed below, the tape control unit has other control circuitry which performs the following functions:

a. Forwards computer commands and addresses to the tape transport unit

b. Interprets computer EOM instructions

c. Responds to SKS instructions

d. Allows a conventional magnetic tape system (such as SDS Model 9248) to be plugged into the Model 9448 auxiliary connector so that it operates compatibly over the same computer buffer channel.

3-155 Control State Counter

3-156 The coordination of all control functions of the tape control unit is provided by the control state counter, CSA-CSC. Operating in conjunction with other control flip-flops and control lines from the computer buffer (in particular, W0, W5, W6, W9, W10, W11), the control state counter declares what MAGPAK is doing at every instant in time. Table 3-1 summarizes the eight control states defined by the CSA-CSC flip-flops.

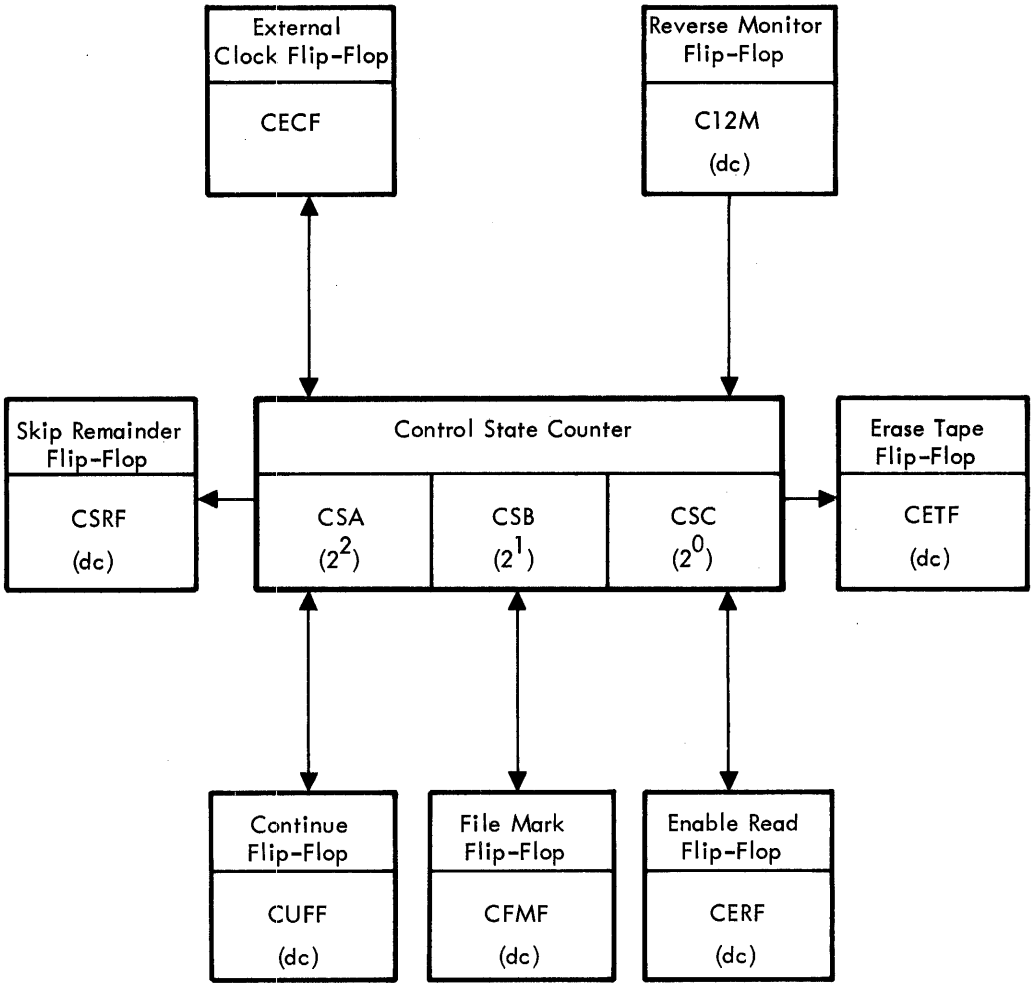


Figure 3-15. Control Logic Block Diagram

Table 3-1. CSA-CSC Control States

Control State	Defined As	Name	Basic Control Activities
CS0	$\overline{CSA}\ \overline{CSB}\ \overline{CSC}$	IDLE-START	Idle--Ready, Forward start motion commands. Erase start gap. Gate out Read
CS1	$\overline{CSA}\ \overline{CSB}$ CSC	PREAMBLE	Write Preamble
CS2	$\overline{CSA}$ CSB $\overline{CSC}$	WRITE	Write characters, output from Computer Buffer
CS3	$\overline{CSA}$ CSB CSC	POSTAMBLE	Write Postamble
CS4	CSA $\overline{CSB}\ \overline{CSC}$	INTERHEAD	Erase gap. Wait for gap to be read
CS5	CSA $\overline{CSB}$ CSC	GAP	Erase gap. Indicate gap to computer
CS6	CSA CSB $\overline{CSC}$	STOP-HALT	Stop tape motion. Erase stop gap. Halt Buffer
CS7	CSA CSB CSC	READ	Read characters, input to Computer Buffer

3-157 External Clock Flip-Flop

3-158 The external clock flip-flop, CECF, is named for its basic function of clocking the computer buffer during information transfers. It actually performs four functions:

a. CECF clocks the computer buffer during write (CS2) in response to WGO1 and in read (CS7) in response to RCP.

b. During CS0, CECF initiates Harvey register timing operations in response to various MAGPAK commands.

c. During CS1 and CS3, CECF is used to time the writing of the preamble and postamble codes.

d. At the beginning of CS4, CS5, and CS6, CECF clears the Harvey register in preparation for binary counting.

3-159 Reverse Monitor Flip-Flop

3-160 The remaining six flip-flops in the control logic section are all of the dc-type (FH19). The reverse monitor flip-flop, C12M, simply remembers the direction in which the tape is commanded to move. It participates in determining the control state sequence.

3-161 Erase Tape Flip-Flop

3-162 The erase tape flip-flop, CETF, is turned on at the beginning of all write or erase operations in CS0. The dc erase signal is supplied by the write logic whenever CETF is on. In write operations, CETF is turned off to start the preamble in CS1 and back on again in CS3 to terminate the postamble.

3-163 Enable Read Flip-Flop

3-164 The enable read flip-flop, CERF, controls the functioning of the read logic. It is turned on when writing begins in CS1 and when reading is to occur in CS7. Reading is disabled by turning off CERF whenever a gap is detected after the preamble has been recognized.

3-165 File Mark Flip-Flop

3-166 The file mark flip-flop, CFMF, is set at the beginning of every read operation and is reset whenever the character in the Harvey register is not a file mark. Thus, if CFMF remains set after a read, a file mark is indicated to the computer. Furthermore, CFMF acts in conjunction with CUFF and CSRF to control the duplicate writing of file marks.

3-167 Continue Flip-Flop

3-168 The continue flip-flop, CUFF, stores the information that a command to continue was given in CS5. This permits CUFF to alter the state sequence so that the tape is not halted. An additional function is performed by CUFF during CS2, the writing state, in that if more than one character is to be written in a record, CUFF detects this and prevents character duplication.

3-169 Skip Remainder Flip-Flop

3-170 The skip remainder flip-flop, CSRF, is used to store the programmed command to ignore remaining characters being read. CSRF then inhibits the clocking of the computer buffer. As mentioned above, CSRF participates in the writing of a file mark in duplicate. A third function

performed by CSRF is to store the information that the tape control unit was the last unit selected. If a conventional magnetic tape system (such as a Model 9248) on the same buffer channel is selected by the computer, CSRF is reset and control is released to the other system. Otherwise, if CSRF is set, the MAGPAK tape control unit seizes control of certain computer responses and locks out the "big tape" system.

3-171 TAPE CONTROL UNIT LOGIC DESCRIPTION

3-172 INTRODUCTION

3-173 A basic knowledge of the logic used in SDS computers is essential to the understanding of logical functions performed by the MAGPAK Tape Control Unit. For purposes of discussion and brevity, many logic equations in the following pragraphs show only part of their gate mechanizations. A complete listing of tape control unit logic equations and a glossary of logic terms are included at the end of this section. Logic diagrams, showing connector and pin locations of signals, are included in section V of this manual.

3-174 The logic described in this section pertains to the operation of a Model 9448 Tape Control Unit used in conjunction with a W-buffer, but the same logic is equally applicable for use with any SDS computer buffer channel.

3-175 Two types of flip-flop circuit modules are used in the tape control unit: the FH19 DC Flip-Flop, and the FH15 Counter Flip-Flop. The first type, the FH19 module, contains six identical flip-flop circuits. Each flip-flop consists simply of two inverting amplifiers, the outputs of which are cross-coupled to the input gates of the opposite amplifier. Inputs to diode control gates, when true, directly set or reset the flip-flop. Thus, in the following equations:

$$sF = XP$$
$$rF = YQ$$

the flip-flop sets as XP goes true and resets as YQ goes true. If X and Y can be true at the same time, then P and Q cannot be simultaneously true or else F would go to an unpredictable state. Furthermore, if X can go true at a time that P is going false, the gating signal XP can produce a slicing condition that might erroneously set F. Accordingly, some input equations to the FH19 are qualified in the tape control unit. For example:

$$sF = XPC$$

in which C is true only at times when X and P are stable. A common dc reset input is also provided on the FH19 which will cause each circuit on the module to reset when it is made false (0 volts).

3-176 The second type of flip-flop module used in the tape control unit, the FH15, is connected in one of two ways: as a repeater, or in a J-K configuration. The repeater connection is described in equations of the form:

$$dF = X$$
$$gF = Y$$
$$cF = W\underline{P}$$

in which the flip-flop takes on the logical value of X (one or zero) whenever P goes from true to false while W is true. It is prevented from changing state if Y is not true. In the J-K configuration, described logically as follows:

$$jF = X$$
$$kF = Y$$
$$cF = W\underline{P}$$

the self-coupled inhibit gates produce steering such that F goes to a one when X is true and Y is false; F goes to a zero when X is false and Y is true, and F goes to its opposite state when both X and Y are true.

3-177 WRITE LOGIC DESCRIPTION

3-178 Write Clock Generator Logic

3-179 The 12 states of the write clock generator are shown in table 3-2; waveforms are shown in figure 3-16. When magnetic tape operations are not addressed by the buffer, the write clock generator is reset to all zeroes:

$$rWCA = rWCB = rWCC = rWCD = \overline{(W11)}\ dc$$

These flip-flops are clocked by the 126-kc reference clock:

$$cWCA = cWCB = cWCC = cWCD = \underline{FC}$$

the least significant three counter stages are permitted to toggle through six-state binary cycles whenever the tape control unit is selected for operation:

$$jWCB = WCC\ WCD$$
$$kWCB = WCD$$
$$jWCC = \overline{WCB}\ WCD$$
$$kWCC = WCD$$
$$jWCD = kWCD = CSG$$
$$CSG = CSA + CSB + CSC + CECF$$

The most significant stage toggles on every sixth reference clock:

$$jWCA = kWCA = WCB\ WCD$$

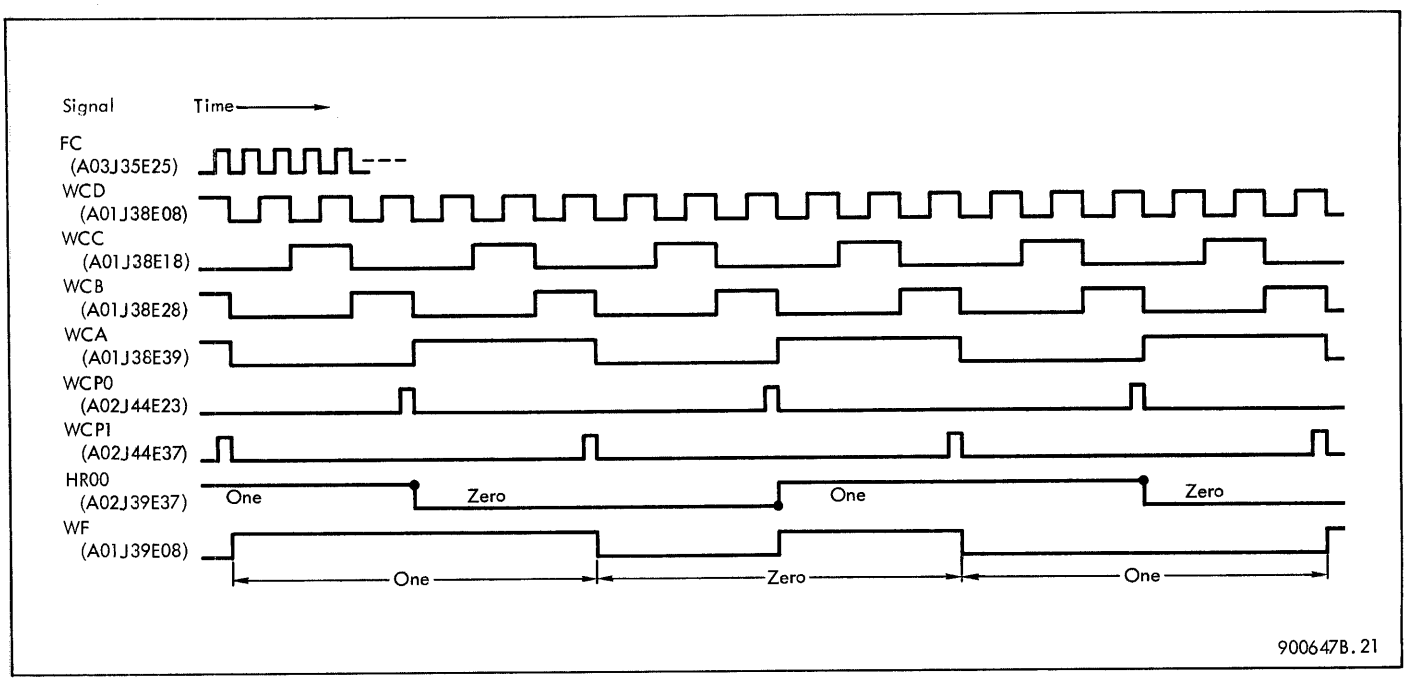


Figure 3-16. Write Clock Generator Waveforms

Table 3-2. Write Clock Generator States

WCA	WCB	WCC	WCD
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1

3-180 Twelve reference clock pulses are thus counted and two symmetrically out-of-phase states are recognized. Write clock phase zero is used for control logic timing, bit shifting and bit strobing during write operations:

$$WCP0 = \overline{WCA}\ WCB\ WCD\ CSG\ FC$$

Write clock phase one is used for the synchronizing transition during writing and to qualify certain dc flip-flop inputs:

$$WCP1 = WCA\ WCB\ WCD\ CSG\ FC$$

3-181 Write Synchronizer Logic

3-182 The seven write synchronizer states are shown in table 3-3; waveforms in figure 3-17. The write synchronizer is held in its all-zero condition when magnetic tape operations are not addressed by the buffer:

$$rWSA = rWSB\ rWSC = \overline{(W11)}\ dc$$

These flip-flops are clocked by the write clock phase zero pulses from the write clock generator:

$$cWSA = cWSB = cWSC = \underline{WCP0}$$

Seven recording bit times are counted by the write synchronizer whenever the 9448 is selected for operation:

$$jWSA = WSB\ WSC\ CSG$$

$$kWSA = WSB\ CSG$$

$$jWSB = WSC\ CSG$$

$$kWSB = (WSA + WSC)\ CSG$$

$$jWSC = (\overline{WSA} + \overline{WSB})\ CSG$$

$$kWSC = WSC\ CSG$$

$$CSG = CSA + CSB + CSC + CECF$$

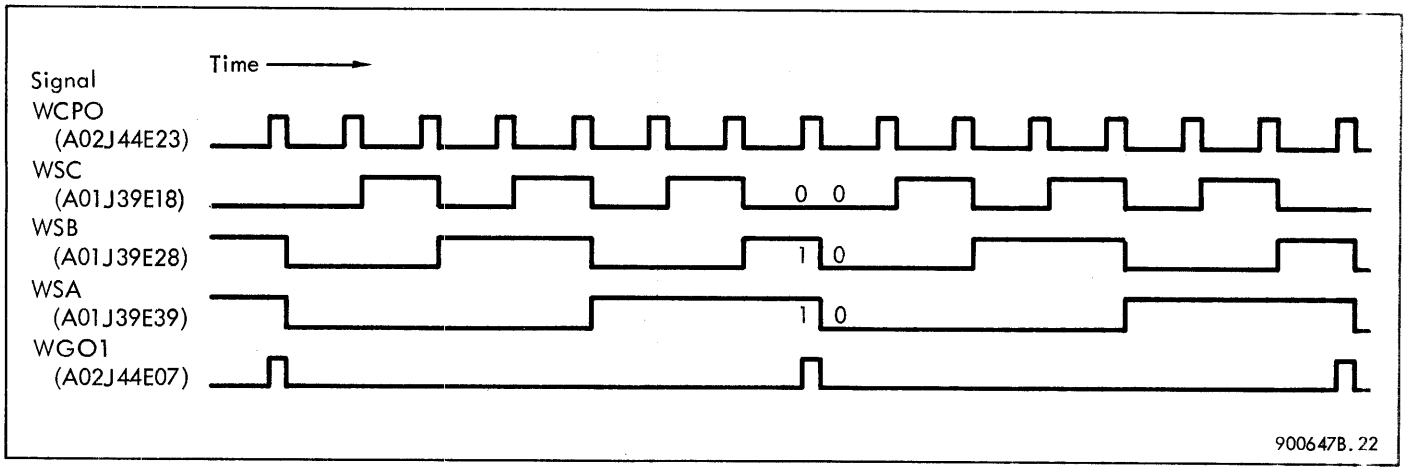


Figure 3-17. Write Synchronizer Waveforms

Table 3-3. Write Synchronizer States

WSA	WSB	WSC
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0

3-183 The write character gate occurs at 1.5 kc and is used for control logic timing and for parallel outputting of characters from the buffer:

$$WGO1 = WSA\ WSB\ WCP0$$

Since WCP0 is true for only one reference clock interval

$$WCP0 = \overline{WCA}\ WCB\ WCD\ CSG\ FC$$

the write character gate is likewise limited in duration to 3.8 microseconds.

3-184 Write Flip-Flop Logic

3-185 The write flip-flop converts the shifting contents of the Harvey register to the phase encoded signal that gets recorded on tape. The flip-flop is permitted to toggle when the 9448 is selected and the buffer calls for a write operation:

$$jWF = kWF = W9\ CSG$$

the clock input establishes the synchronizing transitions at WCP1 time, and when Harvey register zeroes are being written in CS2 the WCP0 signal clocks WF:

$$cWF = \underline{WCP1} + CS2\ \overline{HR00}\ \underline{WCP0} + - - -$$

3-186 The preamble zero is encoded in CS1 under the control of the write synchronizer and CECF, which is reset during the second character time of CS1:

$$cWF = \underline{WCP1} + CS1\ \overline{CECF}\ WSA\ WSB\ \underline{WCP0} + - - -$$

The postamble zero is encoded in CS3 under the control of the write synchronizer and CECF, which is set during the first character time of CS3:

$$cWF = \underline{WCP1} + CS3\ CECF\ \overline{WSA}\ \overline{WSB}\ \overline{WSC}\ \underline{WCP0} + - - -$$

3-187 READ LOGIC DESCRIPTION

3-188 Read Signal Standardizer

3-189 The two flip-flops in the read signal standardizer are forced off whenever the start command is given:

$$rRSF1 = rRSF2 = (\overline{CERF}\ FC)\ dc$$

When reading is enabled (during either read or write operations), the flip-flops are permitted to change states clocked by the 126-kc reference clock:

$$gRSF1 = gRSF2 = CERF$$

$$cRSF1 = cRSF2 = \underline{FC}$$

3-190 A test condition controls the input to RSF1. When not in "test," the read data signal from the selected transport is applied. When in "test," the write data signal is coupled for back-to-back testing:

$$dRSF1 = RDAS\ \overline{TEST} + WDAS\ TEST$$

The output of RSF1 is simply a clocked version of read data square wave signal. It is delayed one reference clock interval (7.9 microseconds) and applied as a shift register-type input to RSF2:

$$dRSF2 = RSF1$$

3-191 Whenever the contents of the two flip-flops are opposite to one another, a transition must have occurred during the previous reference clock interval. Thus, a standardized transition pulse is generated by the following gating:

$$RSF3 = \overline{RSF1}\ RSF2 + RSF1\ \overline{RSF2}$$

The intelligence of the information being read is contained in the time between successive RSF3 pulses.

3-192 Read Decoder

3-193 The time between RSF3 pulses is measured digitally by the read decoder. Four flip-flops, RDA-RDD, are clocked by FC and act as a variable period binary counter, the states of which are shown in figure 3-18. A digital-to-analog converter on the test module gives a staircase voltage proportional to binary state on test point 2 (A01J45E12). Individual waveforms for each flip-flop are shown in figures 3-19 through 3-22. In the absence of transition signals on RSF3, the counter will stall in state 15 (all ones).

$$kRDA = RSF3$$
$$kRDB = RSF3\ RDA + - - -$$
$$kRDC = RSF3\ RDA + - - -$$
$$kRDD = RSF3 + - - -$$

Since RDA is set, the first RSF3 resets the read decoder to zero by the foregoing logic terms. The counter counts up through states 1 and 2.

$$jRDC = (\overline{RSF3} + - - -)\ RDD$$
$$jRDD = \overline{RSF3} + - - -$$
$$kRDD = \overline{RDA} + - - -$$

3-194 Five consecutive states (3 through 7) are then declared by the counter regardless of RSF3.

$$jRDB = (\overline{RDA} + - - -)\ RDC\ RDD$$
$$jRDC = (\overline{RDA} + - - -)\ RDD$$
$$kRDC = (\overline{RDA} + - - -)\ RDD + - - -$$
$$jRDD = \overline{RDA} + - - -$$
$$kRDD = \overline{RDA} + - - -$$

These states bracket the middle of a bit-time and are used to decode zeroes. Counting continues into state 8:

$$jRDA = RDB\ RDC\ RDD$$
$$kRDB = \overline{RDA}\ RDC\ RDD + - - -$$
$$kRDC = (\overline{RDA} + \overline{RDB})\ RDD + - - -$$
$$kRDD = \overline{RDA} + - - -$$

RDA, RDB, RDC, RDD

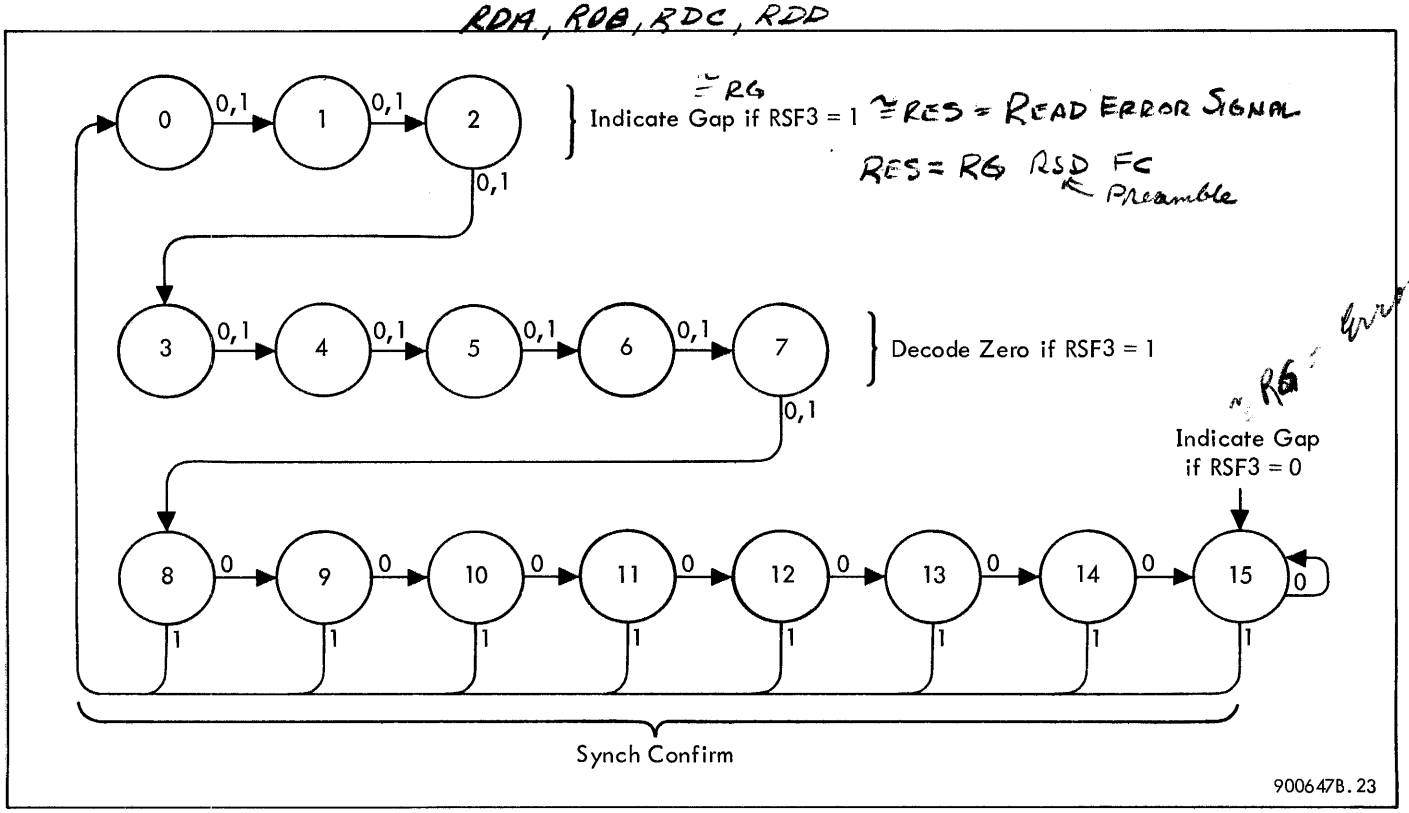


Figure 3-18. Read Decoder State Diagram

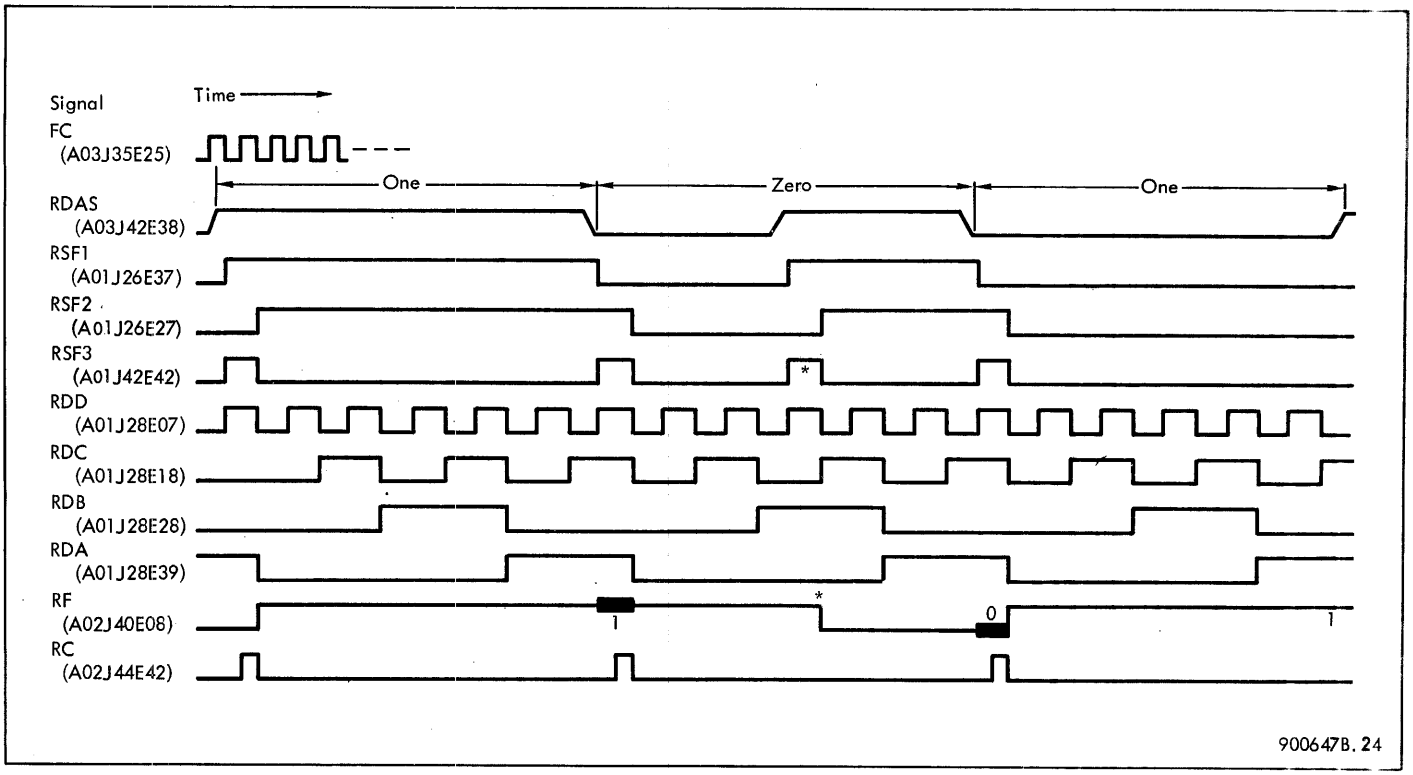


Figure 3-19. Read Decoder Waveforms (Transport Operating at Rated Speed)

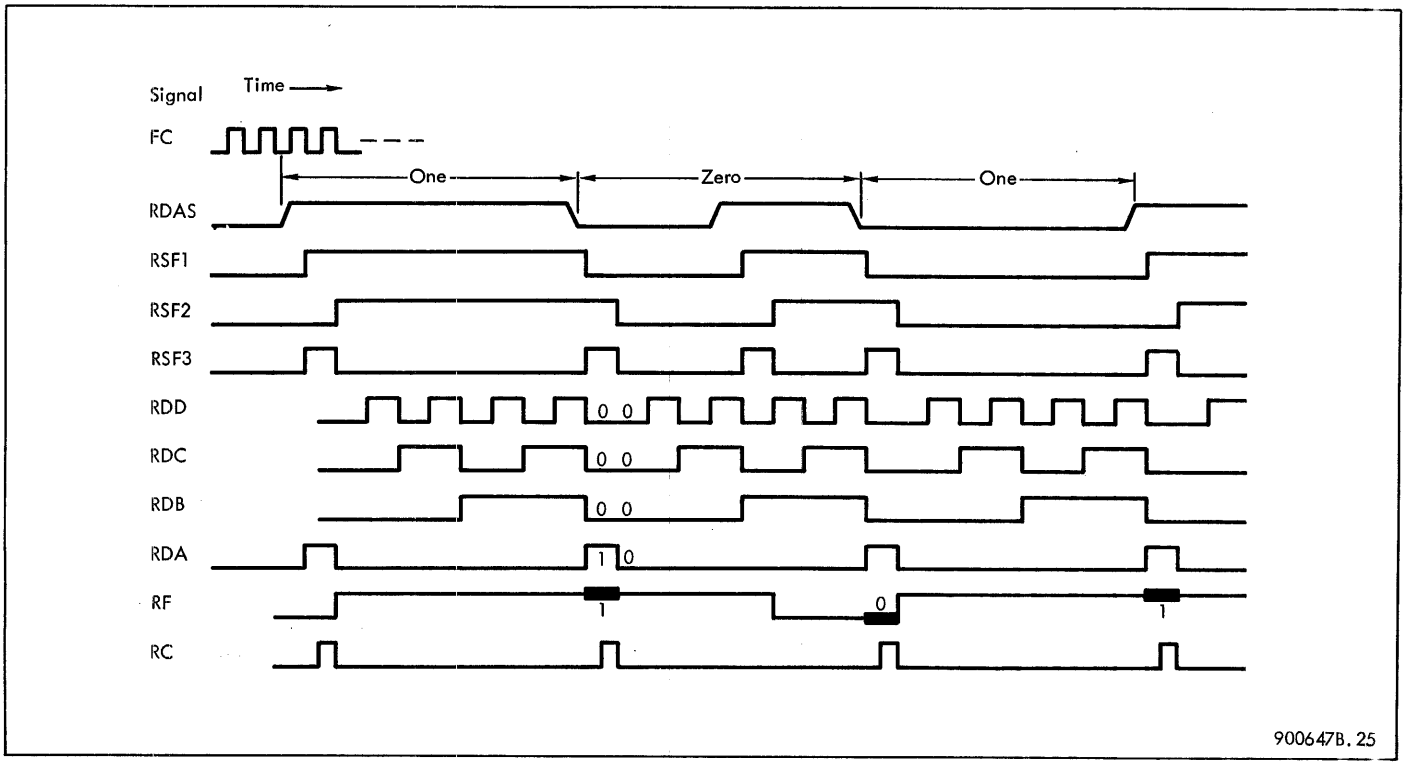


Figure 3-20. Read Decoder Waveforms (Transport Operating at 25% Above Rated Speed)

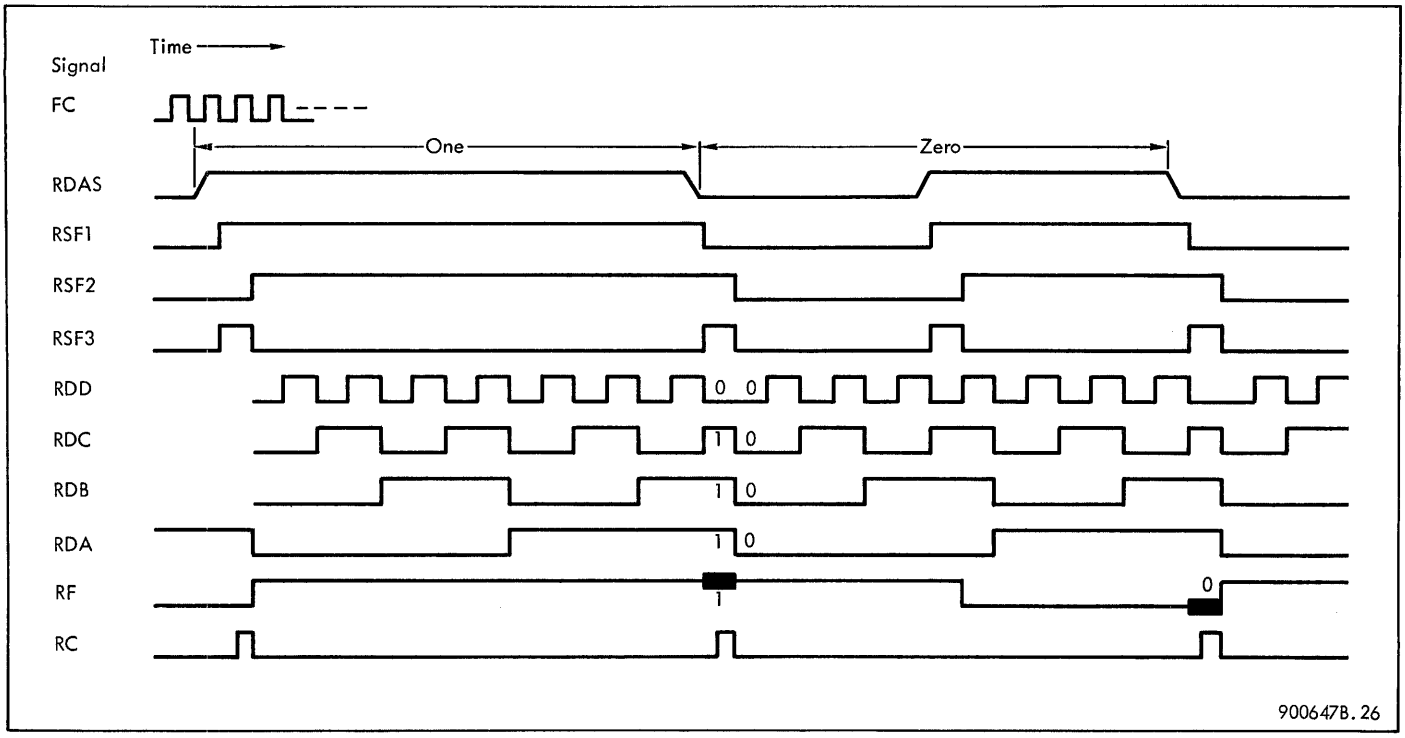


Figure 3-21. Read Decoder Waveforms (Transport Operating at 25% Below Rated Speed)

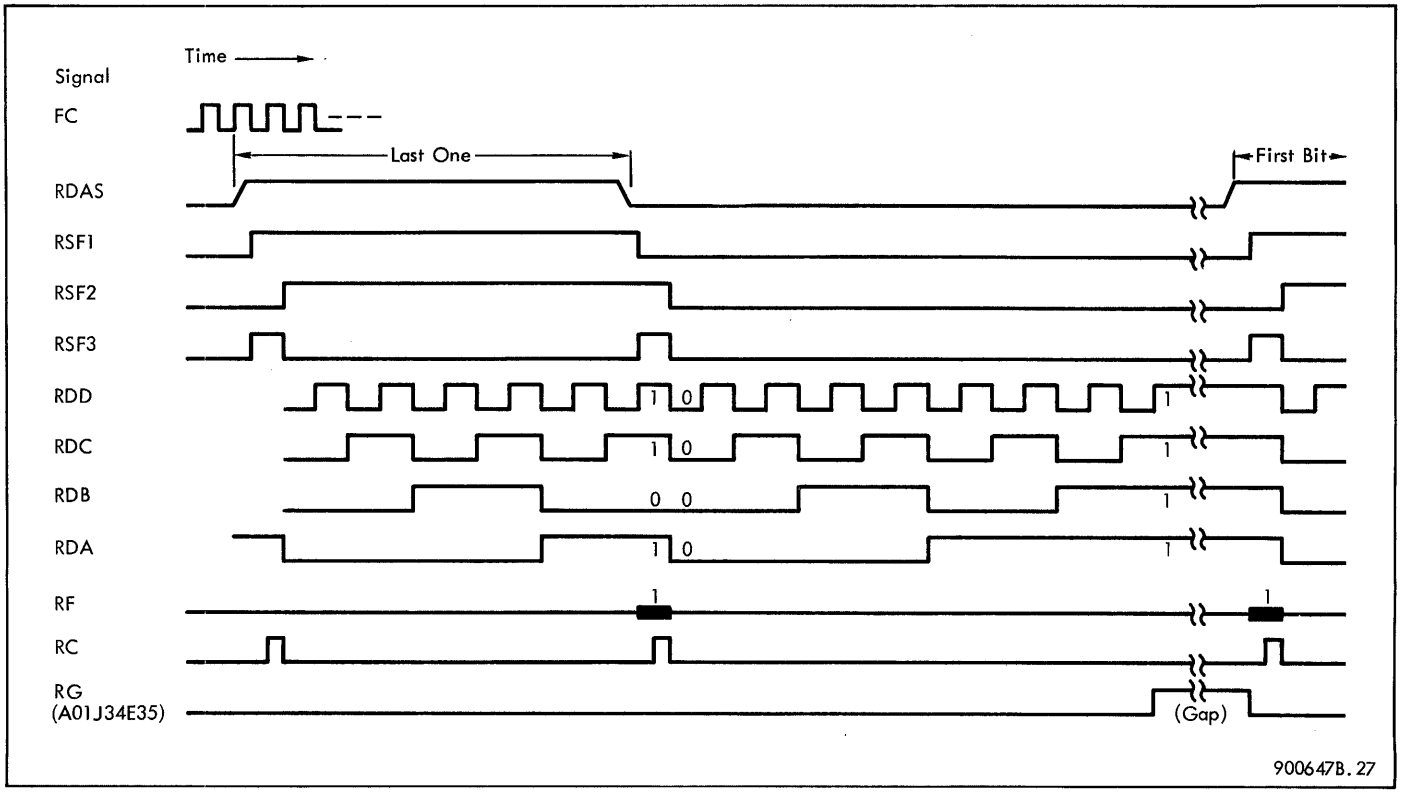


Figure 3-22. Read Decoder Waveforms (Gap Detection)

3-195 Up to eight consecutive states (8 through 15) are then declared by the read decoder, during which synchronism with the data is confirmed. Counting in these states proceeds until an RSF3 signal is generated:

$$jRDB = (\overline{RSF3} + \overline{RDA})\ RDC\ RDD$$

$$kRDB = \overline{RDA}\ RDC\ RDD + - - -$$

$$jRDC = (\overline{RDA} + \overline{RSF3})\ RDD + - - -$$

$$kRDC = (\overline{RDA} + \overline{RDB})\ RDD$$

$$jRDD = \overline{RSF3} + - - -$$

$$kRDD = \overline{RDB} + \overline{RDC} + - - -$$

When the synchronizing transition occurs on RSF3, the counter is returned to zero to process the next bit:

$$kRDA = RSF3$$

$$kRDB = RSF3\ RDA + - - -$$

$$kRDC = RSF3\ RDA + - - -$$

$$kRDD = RSF3 + - - -$$

If no transition occurs before or during state 15, a gap signal is generated and the counter is stalled to wait for the next RSF3 signal.

3-196 The read clock is generated by the read decoder at the time a synchronizing transition is detected during states 8 through 15:

$$RC = RSF3\ RDA\ FC$$

The read gap signal will be generated in states 0 through 2 as a result of detecting an early (spurious) transition:

$$RG = RSF3\ \overline{RDA}\ \overline{RDB}\ (\overline{RDC} + \overline{RDD}) + - - -$$

Furthermore, the read gap signal will be made true if no transition occurs in state 15:

$$RG = \overline{RSF3}\ RDA\ RDB\ RDC\ RDD + - - -$$

3-197 Read Flip-Flop

3-198 The reference clock is used to clock RF:

$$cRF = \underline{FC}$$

Every bit-time the read flip-flop is turned on by the synchronizing transition:

$$jRF = \overline{RDA}\ RSF3$$

If a zero is decoded, RF will be reset by the zero transition which occurs before state 8 in the read decoder:

$$kRF = \overline{RDA}\ RSF3$$

Otherwise, RF remains set throughout the bit time. Thus, the content of RF indicates the logical value (one or zero) of the information being read when examined at the time of the read clock:

$$RC = RSF3\ RDA\ FC$$

3-199 Read Synchronizer

3-200 Bit-times are counted by the read synchronizer so that character synchronism can be maintained throughout a record. Additionally, the read synchronizer detects the preamble and postamble codes and performs a serial parity test on each character. The binary contents of RDA-RDC are converted to analog on the test module; the staircase voltage can be monitored on test point 3 (A01 J45 E22). Refer to figure 3-23 for the discussion of read synchronizer states. Individual flip-flop states can be compared to the waveforms shown in figures 3-24 through 3-27.

3-201 In control state zero, the binary counter portion of the read synchronizer is held in the zero state:

$$rRSA = rRSB = rRSC = (CS0)\ dc$$

The preamble detector is likewise held reset by CS0 or the enable read flip-flop:

$$rRSD = (\overline{CERF}\ FC + CS0)\ dc$$

Before the enable read flip-flop, CERF, is set, both the parity error detector and the postamble detector are initialized to zero:

$$rRSE = (STRT + \overline{CERF}\ FC)\ dc$$

$$rRSF = STRT$$

The set input gates for RSE and RSF are controlled by the enable read flip-flop:

$$gRSE = gRSF = CERF$$

3-202 Four sets of binary states are defined by RDS and RSF. With RSA-RSC reset and with RSD and RSF initially reset, state a_0 is declared in the read synchronizer. Note that the read clock is used as the clock input to all flip-flops in the read synchronizer in the absence of gap:

$$cRSA = cRSB = cRSC = cRSD = cRSE = cRSF = \underline{RC} + RG\ \underline{FC}$$

$$RC = RSF3\ RDA\ FC$$

When a gap signal is generated by the read decoder, the reference clock is gated into the clock inputs.

3-203 The first bit that is decoded regardless of its value lets the count move from a_0 to a_1

$$jRSC = (\overline{RSA} + \overline{RSB})\ \overline{RG}$$

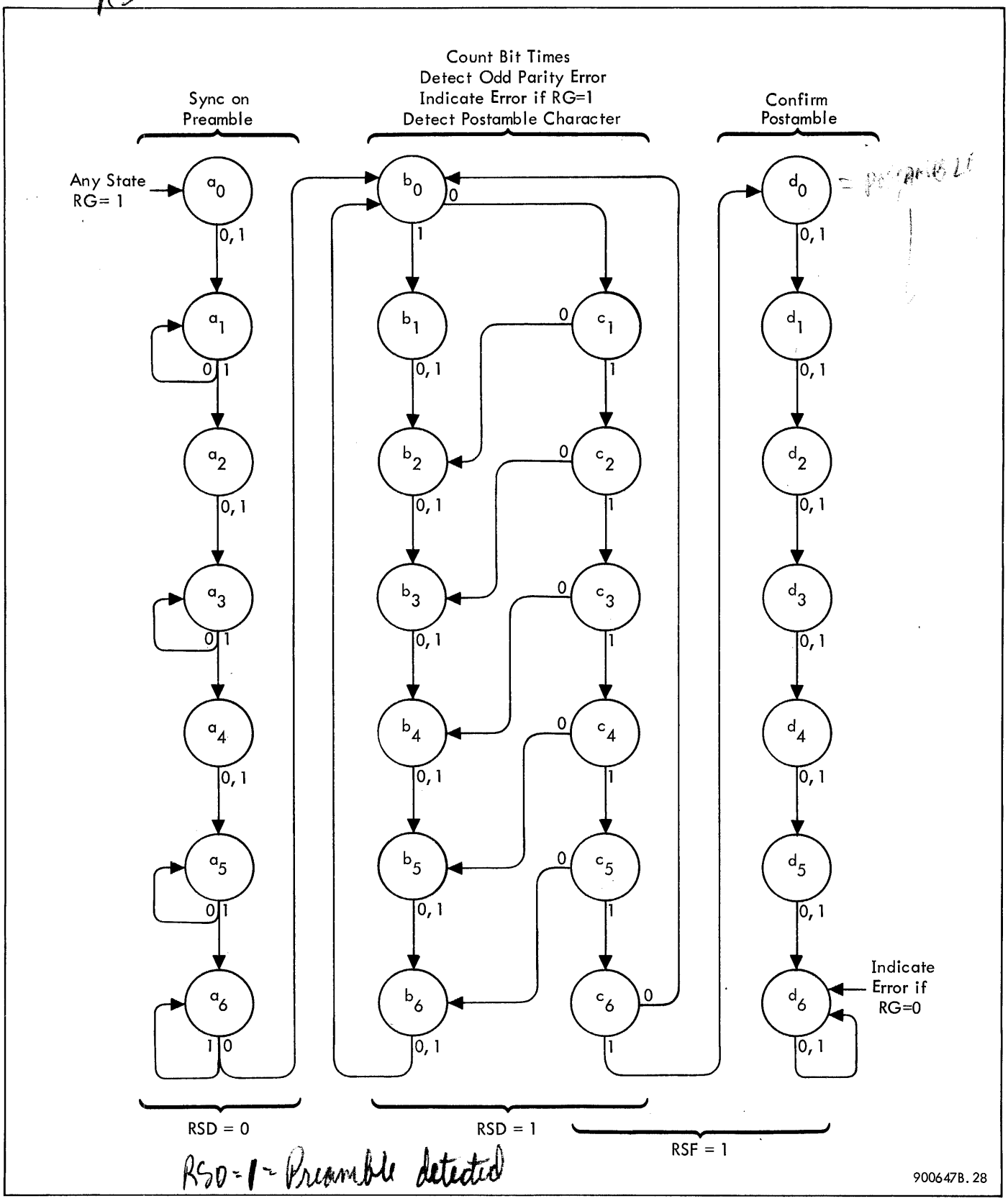


Figure 3-23. Read Synchronizer State Diagram

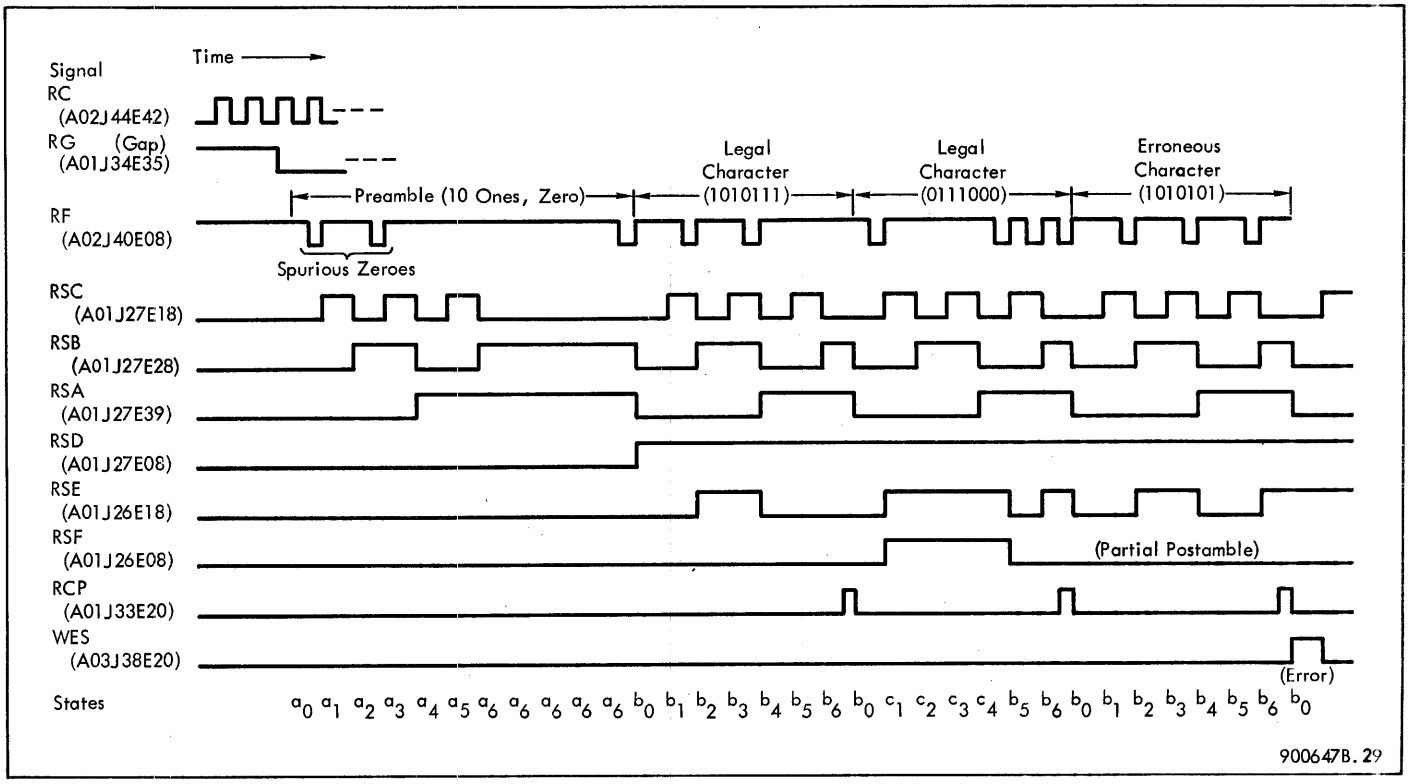


Figure 3-24. Read Synchronize Waveforms (Normal Postamble Detection and Parity Detection)

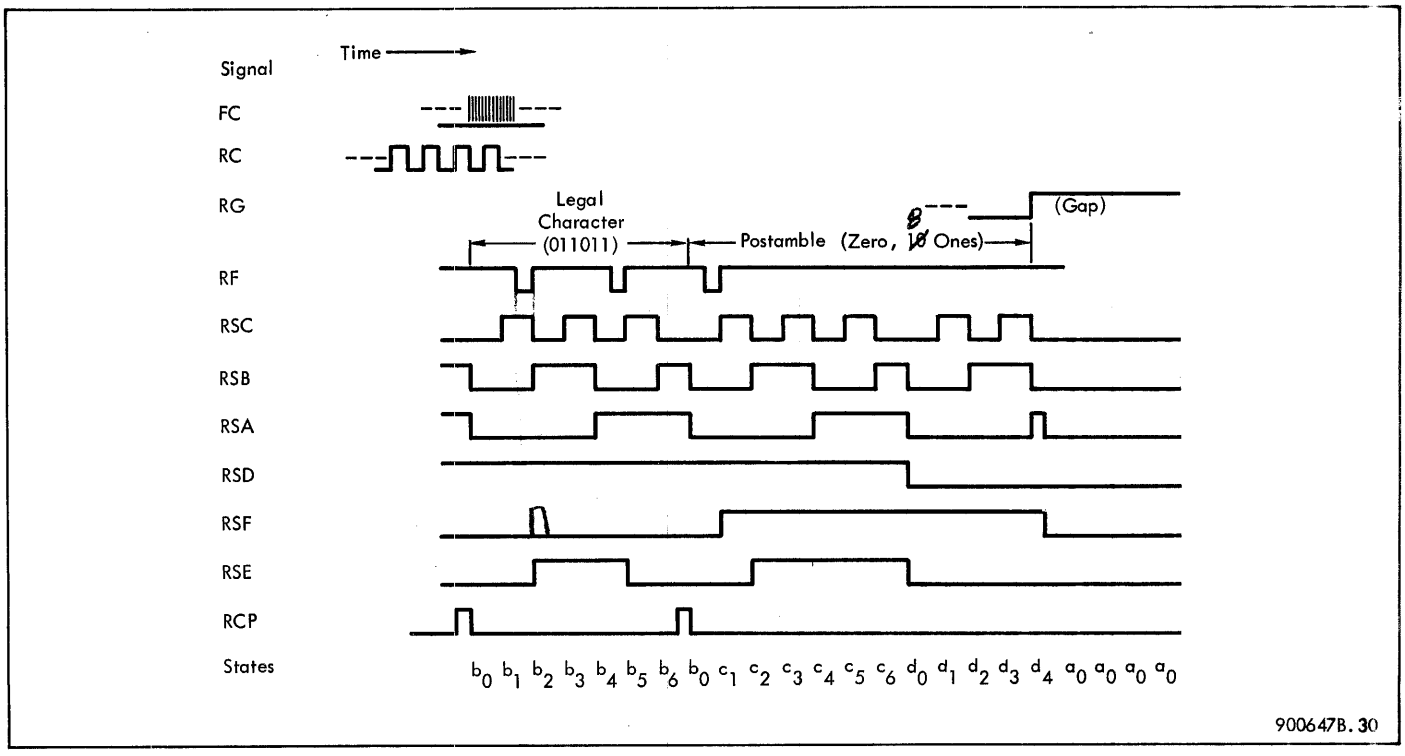


Figure 3-25. Read Synchronizer Waveforms (Normal Postamble Detection)

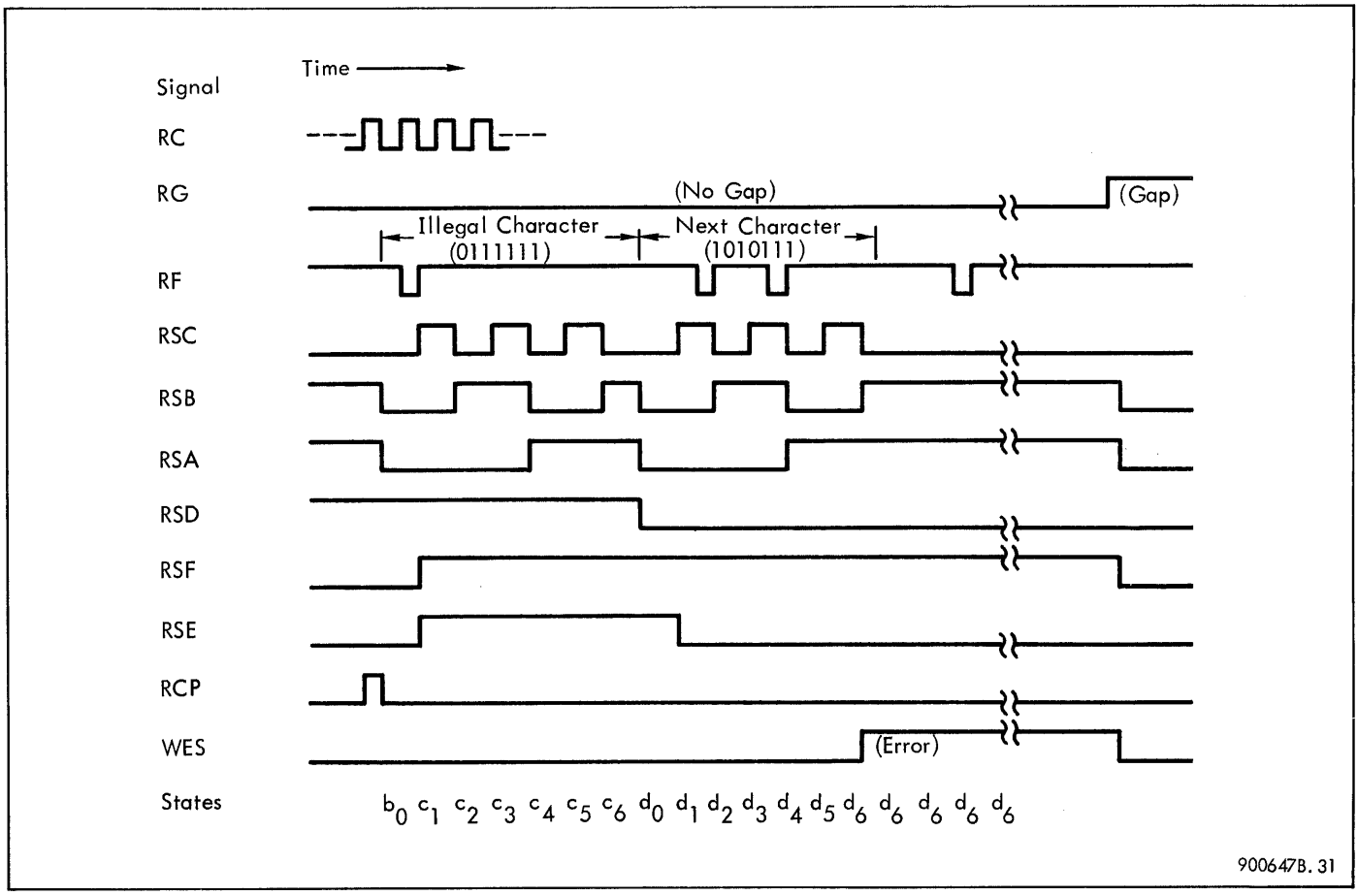


Figure 3-26. Read Synchronizer – Detector Waveforms (Premature Postamble Detection)

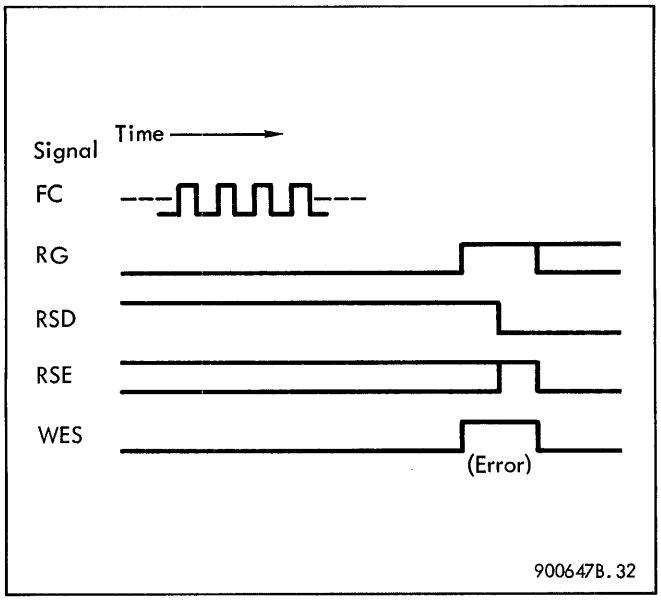


Figure 3-27. Read Synchronizer – Detector Detailed Waveforms (Premature Gap)

When a gap occurs in any state, the counter returns to all zeroes:

$$kRSA = RG + - - -$$

$$kRSB = RG + - - -$$

$$kRSC = RG + - - -$$

In state a_1, the counter will stall until a legal preamble one is decoded:

$$jRSB = RSC\ (RSD + RSF + RF)\ \overline{RG}$$

$$kRSC = RSC\ (RF + - - -) + - - -$$

The arrival of a one lets the counter proceed to a_2 and then a_3 regardless of the content of RF:

$$jRSC = (\overline{RSA} + \overline{RSB})\ \overline{RG}$$

3-204 This process continues, while the read decoder confirms every other bit as a preamble one until state a_6 is reached. A certain tolerance to the incoming bits is thus

provided so that the read amplifiers may stabilize while emerging from the gap. Approximately six of the eight preamble ones will normally place the read synchronizer into state a_6 where it will stall waiting for the preamble zero:

$$kRSA = \overline{RF}\ RSB\ \overline{RSF} + - - -$$

$$kRSB = \overline{RF}\ RSA\ \overline{RSF} + - - -$$

Both RSA and RSB are reset by the preamble zero as indicated above, and the preamble detector is set:

$$jRSD = \overline{RF}\ RSA\ RSB\ \overline{RSF}\ \overline{RG}$$

3-205 With RSA-RSC reset and RSD set, the read synchronizer is in state b_0. The counter proceeds to cycle through seven binary states:

$$jRSA = RSB\ RSC\ (RSD + - - -)\ \overline{RG}$$

$$kRSA = RSB\ RSD + - - -$$

$$jRSB = RSC\ (RSD + - - -)\ \overline{RG}$$

$$kRSB = RSC\ (RSD + - - -)\ \overline{RG} + RSA\ RSD + - - -$$

$$jRSC = (\overline{RSA} + \overline{RSB})\ \overline{RG}$$

$$kRSC = RSC\ (RSD + - - -) + - - -$$

If the first bit of any character is a one, the postamble is not to be detected and the counting cycles from b_0 to b_1 and so forth to b_6 and then back to b_0. During b_0, a zero may be present and the postamble detector is turned on:

$$jRSF = \overline{RF}\ \overline{RSA}\ \overline{RSB}\ \overline{RSC}\ RSD\ \overline{RG}$$

3-206 With RSF set, the read synchronizer is in state c_1 and will proceed to c_2 if a one is detected. If ones continue to come in following the first zero, the postamble detector remains set and the counting continues toward c_6. Any time that a zero is found after the first bit, RSF is reset:

$$kRSF = \overline{RF}\ RSD\ CERF$$

Thus, any non-preamble code will take the read synchronizer back to one of the b states. When state c_6 is reached, the condition of the read flip-flop determines if a postamble character is being read. A zero in RF during state c_6 resets RSF, and since RSA-RSC are also reset at this time, the read synchronizer returns to state b_0 to process another character. If RF contains a one in state c_6, the first seven bits of the postamble are assumed to have been read, and RSD is reset:

$$kRSD = RF\ RSA\ RSB\ RSF + - - -$$

3-207 Since RSF is still set, the read synchronizer is placed in state d_0. The counter continues to meter out bit-times:

$$jRSA = RSB\ RSC\ (RSF + - - -)\ \overline{RG}$$

$$jRSB = RSC\ (RSF + - - -)\ \overline{RG}$$

$$kRSB = RSC\ (RSF + - - -)\ \overline{RG}$$

$$jRSC = (\overline{RSA} + \overline{RSB})\ \overline{RG}$$

$$kRSC = RSC\ (RSF + - - -) + - - -$$

If a true postamble code is being read, six of its ones were processed in states c_1 through c_6, and only two more ones are present on the tape before gap should be detected. Under normal conditions, therefore, the RG signal should be generated in state d_2 or d_3. This causes the counter to reset:

$$kRSA = RG + - - -$$

$$kRSB = RG + - - -$$

$$kRSC = RG + - - -$$

On the other hand, if the postamble character were prematurely detected in the record, at least nine more bits (the true postamble) would follow it, and the counter would arrive at state d_6 without an RG to reset it. Accordingly, state d_6 is used for part of the read error detection.

3-208 The parity error detector is active during the reading of each character of the record. It is used to count zeroes instead of ones. Inasmuch as each character is recorded with odd parity, the number of zeroes read back should be even, and RSE is normally off during state b_0 at which time it is acted upon as follows:

$$jRSE = RSD\ \overline{RF}\ \overline{RG}$$

$$kRSE = CERF\ \overline{RF}\ RSD$$

During this bit-time and all the subsequent bit-times that RSD is one, RSE is toggled by zeroes in RF. Its contents are examined by the read error logic in state b_0.

3-209 The primary output of the read synchronizer is the read character pulse:

$$RCP = RSA\ RSB\ RSD\ (\overline{RSF} + \overline{RF})\ RC$$

This signal occurs simultaneously with the last read clock of each non-postamble character.

3-210 There are three elements in the read error signal supplied by the read synchronizer to the control logic. The gap in data signal occurs in states b_0-b_6, c_1-c_6:

$$RES = RG\ RSD\ FC + - - -$$

A parity error is indicated if RSE is on during state b_0:

$$RES = RSE\ \overline{RSA}\ \overline{TSB}\ \overline{RSC}\ \overline{RSF} + - - -$$

The occurrence of a premature postamble is detected if state d_6 is reached:

$$RES = RSA\ RSB\ \overline{RSD}\ RSF + - - -$$

3-211 HARVEY REGISTER LOGIC DESCRIPTION

3-212 A seven-stage Harvey register is included in the tape control unit to perform the functions of parallel-to-serial conversion and serial-to-parallel conversion, and also to provide timing signals for starting, stopping, and continuing sequences.

3-213 The basic timing-sharing is achieved by four gates: SFG, SRG, SPG, and CBG. Either the shift forward gate or shift reverse gate may be true during CS2 or CS7, the writing and reading control states respectively:

$$SFG = CS27\ \overline{C12M}\ \overline{CECF}$$

$$SRG = CS27\ C12M\ \overline{CECF}$$

The C12M flip-flop remembers the direction of tape motion. The external clock flip-flop CECF is used for parallel transfers to the Harvey register and must be reset for serial shifting. The shift parallel gate is true only during writing and then only when a character is being clocked by CECF from the buffer:

$$SPG = CS2\ CECF$$

In control states 0, 4, 5, 6, the Harvey register is converted to a binary counter under the control of the count binary gate:

$$CBG = CS0 + (CS4 + CS56)\ \overline{CECF}$$

In control states 4, 5, 6, the external clock flip-flop is used to clear the Harvey register prior to counting; therefore, CECF must be reset to enable CBG.

3-214 Time-shared clocking of the Harvey register is accomplished by two generalized pulse gates, SSP and SPP. The shift serial pulse is derived from the write clock generator during writing:

$$SSP = CS2\ \underline{WCP0} + - - -$$

During reading, the read decoder supplies the read clock for shifting:

$$SSP = CS7\ \underline{RC} + - - -$$

The shift parallel pulse is controlled primarily by CECF, and the logic can be expanded as follows:

$$SPP = \overline{CS0}\ \overline{CS7}\ CECF\ FC$$
$$= (CS1 + CS2 + CS3 + CS4 + CS5 + CS6)\ CECF\ \underline{FC}$$

Using this expanded form, it should be noted first that the Harvey register is not active in CS1 or CS3. In CS2, the SPP is used to clock characters from the computer buffer into the HR. In the beginning of control states 4, 5, 6, and CECF is on, and the SPP is used to reset the Harvey register to all zeroes prior to binary counting.

3-215 The seven stages in the Harvey register are all connected as repeaters. A character is transferred in parallel from the computer buffer as follows:

$$dHR00 = SPG\ RP + - - -$$

$$dHR01 = SPG\ R1 + - - -$$

$$dHR02 = SPG\ R2 + - - -$$

$$dHR03 = SPG\ R3 + - - -$$

$$dHR04 = SPG\ R4 + - - -$$

$$dHR05 = SPG\ R5 + - - -$$

$$dHR06 = SPG\ R6 + - - -$$

$$cHR00 = \underline{SPP} + - - -$$
$$\vdots$$
$$cHR06 = \underline{SPP} + - - -$$

3-216 Shifting forward is performed under the control of the following logic:

$$dHR00 = SFG\ HR01 + - - -$$

$$dHR01 = SFG\ HR02 + - - -$$

$$dHR02 = SFG\ HR03 + - - -$$

$$dHR03 = SFG\ HR04 + - - -$$

$$dHR04 = SFG\ HR05 + - - -$$

$$dHR05 = SFG\ HR06 + - - -$$

$$dHR06 = SFG\ HRIN$$

$$cHR00 = \underline{SPP} + - - -$$
$$\vdots$$
$$cHR06 = \underline{SPP} + - - -$$

3-217 In order to duplicate file mark codes, it is necessary to preserve the contents of the Harvey register by recirculation:

$$HRIN = W9\ HR00 + - - -$$

During read/scan forward operations the HR06 receives the output of the read flip-flop serially:

$$HRIN = \overline{W9}\ RF + - - -$$

3-218 Shifting for scan reverse operations is performed under the control of the following logic:

$$dHR00 = SRG\ RF + - - -$$

$$dHR01 = SRG\ HR00 + - - -$$

$$dHR02 = SRG\ HR01 + - - -$$

$$dHR03 = SRG\ HR02 + - - -$$

$$dHR04 = SRG\ HR03 + - - -$$

$$dHR05 = SRG\ HR04 + - - -$$

$$dHR06 = SRG\ HR05 + - - -$$

$$cHR00 = \underline{SSP} + - - -$$

$$\vdots$$

$$cHR06 = \underline{SSP} + - - -$$

3-219 For counting in binary, the repeater inputs are connected to self-terms for steering:

$$dHR00 = CBG\ \overline{HR00} + - - -$$

$$dHR01 = CBG\ \overline{HR01} + - - -$$

$$dHR02 = CBG\ \overline{HR02} + - - -$$

$$dHR03 = CBG\ \overline{HR03} + - - -$$

$$dHR04 = CBG\ \overline{HR04} + - - -$$

$$dHR05 = CBG\ \overline{HR05} + - - -$$

$$dHR06 = CBG\ \overline{HR06} + - - -$$

The clock inputs are connected for forward transition binary counting clocked at the least significant stage by WGO1 (1.6 kc):

$$cHR00 = CBG\ \underline{WGO1}$$

$$cHR01 = CBG\ \underline{HR00}$$

$$cHR02 = CBG\ \underline{HR01}$$

$$cHR03 = CBG\ \underline{HR02}$$

$$cHR04 = CBG\ \underline{HR03}$$

$$cHR05 = CBG\ \underline{HR04}$$

$$cHR06 = CBG\ \underline{HR05}$$

3-220 For resetting the Harvey register prior to counting at the beginning of CS4, CS5, or CS6, the external clock flip-flop is set making SFG, SRG, and CBG zero. Since SPG is qualified by CS2, it is also zero so that all repeater inputs are false. The SPP is made true, however, so the Harvey register gets a clock pulse to reset it to all zeroes.

3-221 Since Harvey register logic requires inverter inputs to all stages, each term is mechanized in complementary form. This necessitates a control term which, though it does not appear in the equations, prevents erroneous input terms from appearing. This is called the Harvey register gate:

$$HRG = \overline{SFG}\ \overline{SRG}\ \overline{SPG}\ \overline{CBG}$$

The HRG participates in the mechanization as indicated in the following example:

$$dHR00 = SFG\ HR01 + SRG\ RF + SPG\ RP + CBG\ \overline{HR00}$$

$$= \overline{SFG\ HR01 + SRG\ \overline{RF} + SPG\ \overline{RP}} + \overline{CBG\ HR00 + HRG}$$

3-222 CONTROL LOGIC DESCRIPTION

3-223 Introduction

3-224 The functions performed by the tape control unit in each control state are summarized in figure 3-35 and table 3-4 (located near the end of this section). Test Point 1 (A01 J45 E02) is the output of a digital-to-analog converter which can be used to monitor the control states.

3-225 Selection and Starting (CS0)

3-226 A MAGPAK tape process is selected and started by executing an appropriate EOM command. A summary of these commands is given in section II of this manual. The following description begins with MAGPAK not selected by the buffer. It is held in CS0:

$$rCSA = rCSB = rCSC = (\overline{W11}\ \overline{STRT})\ dc$$

$$CS0 = \overline{CSA}\ \overline{CSB}\ \overline{CSC}$$

The IDLE-READY state is maintained because CECF is held reset:

$$rCECF = (\overline{W11}\ \overline{STRT})\ dc$$

A generalized start command is generated for tape commands addressed through the buffer:

$$STRT = BUC\ \overline{C17}\ C20$$

The appropriate tape motion control signal is submitted to the tape transport unit electronics. Forward motion is activated by T12S:

$$T12S = STRT\ \overline{C12}\ Q2$$

and reverse motion is activated by S12T:

$$S12T = STRT\ C12\ Q2$$

The tape reverse monitor flip-flop is set to remember reverse operations. It is held reset prior to buffer selection:

$$sC12M = STRT\ C12$$

$$rC12M = \overline{W11}$$

3-227 The least significant octal digit in the computer C-register is decoded into logical tape unit addresses and forwarded to the tape transport unit:

$$LLT0 = \overline{C21}\ \overline{C22}\ \overline{C23}$$
$$\vdots$$
$$LLT7 = C21\ C22\ C23$$

The tape transport unit selects the appropriate transport according to the UNIT SELECT switch position. The TSA or TSB dc flip-flop for the selected transport is set for forward or reverse motion, respectively. As selection is established, the tape transport unit returns a select signal over the SELS bus. The 9448 departs IDLE-READY when the command loop is closed.

$$¡CECF = CS0\ \overline{STRT}\ SELS + - - -$$

$$cCECF = \underline{FC}$$

With CECF set as a result of selection, the write clock generator starts counting:

$$¡WCD = kWCD = CSG$$

$$cWCD = \underline{FC}$$

$$CSG = CECF + - - -$$

The buffer is addressed for tape unit operation, so the write synchronizer is allowed to count:

$$rWSA = rWSB = rWSC = (\overline{W11})\ dc$$

These two counters produce WGO1 pulses at 1.5 kc:

$$WCP0 = \overline{WCA}\ WCB\ WCD\ CSG\ FC$$

$$WGO1 = WSA\ WSB\ WCP0$$

The Harvey register counts forward in binary in control state 0 clocked by WGO1 (1.5 kc):

$$CBG = CS0 + - - -$$

$$cHR00 = CBG\ \underline{WGO1} + - - -$$

3-228 Certain safety features are mechanized in the tape control unit and should be introduced here. If for any reason a start command is not honored by the 9446 Tape Transport Unit, the buffer is halted. Thus, if a reverse command is given at the beginning of tape or if the unit is not ready, the 9446 refuses to select and SELS is not made true. This condition is detectable if SELS is not true after Q2 in the computer has elapsed during a start command:

$$\overline{Whs} = \overline{\overline{SELS}\ AANS\ \overline{Q2}\ STRT} + - - -$$

The address acknowledge signal AANS is present to preclude halting if no transport UNIT SELECT switches are set to the value corresponding to the start command address (C21-C23). AANS is included above because of the requirements of the auxiliary control logic.

3-229 Logic is also provided to halt the buffer if the 9446 transport deselects in CS1, CS2, CS3, CS4, or CS7:

$$\overline{Whs} = \overline{\overline{CS0}\ \overline{CS56}\ \overline{SELS}\ \overline{TEST}} + - - -$$

$$CS56 = CS5 + CS6$$

Accordingly, in a scan reverse or erase reverse, if the beginning of tape clear space is encountered, SELS will go false and the buffer is halted. Any other condition that disqualifies SELS in the 9446 will likewise produce a halt signal.

3-230 Write or Erase Forward (CS0)

3-231 The write tape control signal is generated and sent to the transport electronics to enable the selected write amplifier to apply write current:

$$WRTS = W9\ SELS$$

The erase tape flip-flop is turned on:

$$sCETF = CS0\ W9\ W11\ WCP1 + - - -$$

Control state 0 is maintained for 36.0 milliseconds for write or erase forward (see figures 3-28 and 3-29). This allows time for the forward pressure roller to engage the tape, accelerate it to 7.5 ips, and move the nominal 0.225 inch required to complete the erasure of the gap. To accomplish the necessary delay, the start gap delay is decoded from the Harvey register:

$$STGD = HR05\ HR04\ HR02\ HR00\ WGO1$$

Following the 36.0-millisecond delay, the 9448 enters control state 1 to write the preamble:

$$¡CSC = CS0\ W9\ STGD + - - -$$

$$cCSC = \underline{WGO1}$$

$$CS1 = \overline{CSA}\ \overline{CSB}\ CSC$$

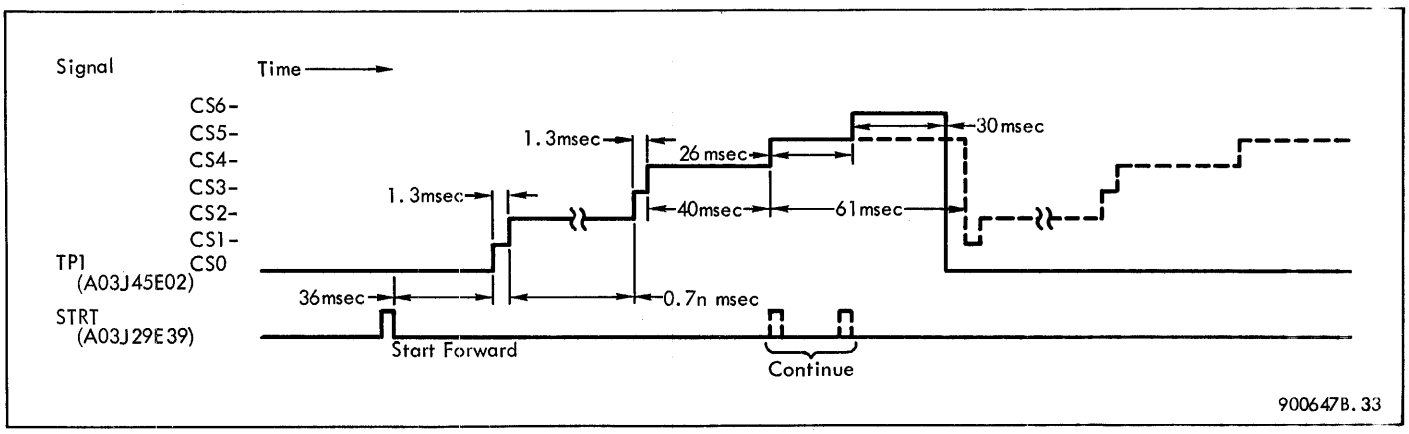


Figure 3-28. Write Forward Control State Sequence

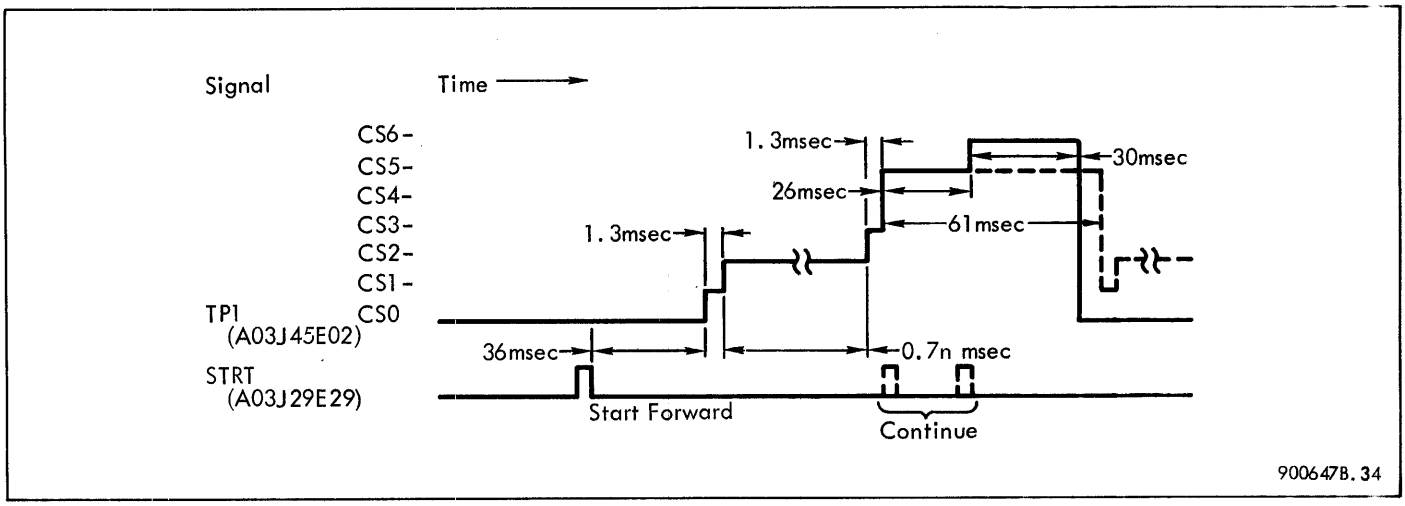


Figure 3-29. Erase Forward Control State Sequence

3-232 Write or Erase Forward (CS1)

3-233 Reading is enabled:

$$sCERF = CS13 + - - -$$

Control state 1 lasts for 14 bit-intervals under the control of CECF which is left set from CS0. The erase tape flip-flop is reset after the fifth bit-interval in a write operation:

$$rCETF = CS1\ \overline{W10}\ WSA\ WSC\ WCP1$$

The write flip-flop is gated onto the write data bus:

$$WDAS = \overline{CETF}\ WF$$

It is toggles by write clock phase 1 to lay down synchronizing transitions for the preamble ones:

$$jWF = kWF = W9\ CSG$$

$$cWF = \underline{WCP1} + - - -$$

At the seventh bit-interval, WGO1 resets CECF for the second character time of CS1:

$$kCECF = CS13\ WGO1 + - - -$$

$$CS13 = \overline{CSA}\ CSC$$

Six more ones are written by WF, and the preamble zero transition is inserted in the last recorded bit:

$$cWF = \underline{WCP1} + CS1\ \overline{CECF}\ WSA\ WSB\ \underline{WCO0} + - - -$$

3-234 At the same time, the 9448 goes to control state 2 for writing the record or for timing the erasing of the record:

$$jCSB = CS1\ \overline{CECF} + - - -$$

$$kCSC = CS1\ \overline{CECF} + - - -$$

$$cCSB = cCSC = \underline{WGO1}$$

$$CS2 = \overline{CSA}\ CSB\ CSC$$

As the 9448 enters CS2, the external clock flip-flop is set to request the first character from the buffer:

$$jCECF = CS13\ WGO1 + - - -$$

$$cCECF = \underline{FC}$$

While in CS1, the continue flip-flop, skip-remainder flip-flop, and file mark flip-flop are all initialized to zero:

$$rCUFF = CS13 + - - -$$

$$rCSRF = \overline{CSB}\ WCP1 + - - -$$

$$rCFMF = CS13 + - - -$$

$$CS13 = \overline{CSA}\ CSC$$

3-235 Write or Erase Forward (CS2)

3-236 In control state 2, the actual record is written (or erased). The external clock flip-flop, which was set for the first character in CS1, provides the clock to the computer buffer:

$$\overline{Ecw} = \overline{CS27\ CERF\ \overline{CSRF}\ CECF} + - - -$$

$$CS27 = CS2 + - - -$$

Each character is transferred to the Harvey register in parallel:

$$dHR00 = SPG\ RP + - - -$$

$$dHR01 = SPG\ R1 + - - -$$

$$\vdots$$

$$dHR06 = SPG\ R6 + - - -$$

$$cHR00 = \underline{SPP} + - - -$$

$$\vdots$$

$$cHR06 = \underline{SPP} + - - -$$

$$SPG = CS2\ CECF$$

$$SPP = \overline{CS0}\ \overline{CS7}\ CECF\ \underline{FC}$$

The buffer responds to the clock by making W6 true, which resets CECF:

$$kCECF = CS27\ W6 + - - -$$

$$cCECF = \underline{FC}$$

$$CS27 = CS2 + - - -$$

With CECF reset, the Harvey register starts shifting clocked by WCP0:

$$dHR00 = SFG\ HR01 + - - -$$

$$dHR01 = SFG\ HR02 + - - -$$

$$\vdots$$

$$dHR05 = SFG\ HR06 + - - -$$

$$cHR00 = \underline{SSP} + - - -$$

$$\vdots$$

$$cHR06 = \underline{SSP} + - - -$$

$$SFG = CS27\ C12M\ CECF$$

$$SSP = CS2\ WCP0 + - - -$$

$$CS27 = CS2 + - - -$$

The serialized character appearing in HR00 is encoded by WF:

$$kWF = W9\ CSG$$

$$cWF = \underline{WCP1} + CS2\ \overline{HR00}\ \underline{WCP0} + - - -$$

In write operations, WF is applied on the write data bus to the tape transport unit electronics. An erase operation sustains a dc logical zero:

$$WDAS = \overline{CETF}\ WF$$

3-237 In a normal write or erase process, the foregoing sequence is repeated for each output character. When the file mark code is written, however, only one character is supplied by the buffer. A combination of idiosyncrasies in conventional recording on SDS magnetic tape unit (such as Models 9246 and 9146), causes the reading of the file mark to appear as two identical characters. (In particular, the buffer is arranged so that it will not honor a gap signal until two or more characters are read. The longitudinal, even-parity check character in conventional formats is therefore read as the second character in a file mark.) Inasmuch as MAGPAK must be compatible with programs written for these other transports, the file mark character must be recorded in duplicate for subsequent reading operations.

3-238 The normal write sequence (more than one character) is characterized by the fact that W5 in the buffer is false following all character transmissions except the last (see figure 3-30).

This fact is remembered by the continue flip-flop:

$$sCUFF = CS2\ \overline{W5}\ WSB\ WCP1 + - - -$$

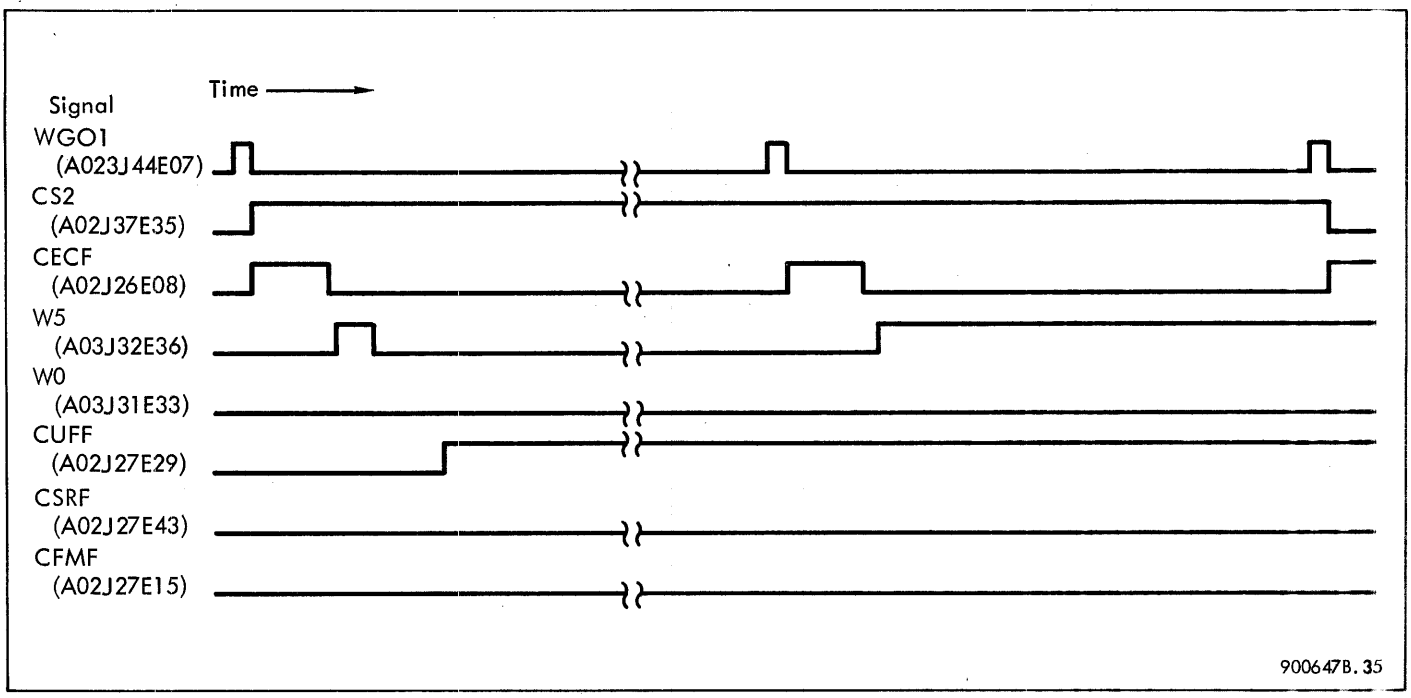


Figure 3-30. Normal Write Sequence

The external clock flip-flop is set after the serial recording of each character by WGO1:

$$jCECF = CS2\ (CUFF + - - -)\ WGO1 + - - -$$

$$cCECF = \underline{FC}$$

This calls for the transmission of the next character from the buffer, and the sequence is repeated as required.

3-239 In the file mark write sequence, on the other hand, W5 will be true after the first character is transmitted and CUFF is left reset (see figure 3-31). CSRF is set at the end of the first character time by the leading edge of WGO1:

$$sCSRF = CS2\ \overline{CUFF}\ WGO1 + - - -$$

With CSRF set, the external clock flip-flop cannot get through to the buffer:

$$\overline{Ecw} = \overline{CS27\ CERF\ \overline{CSRF}\ CECF} + - - -$$

The file mark code was recirculated in the Harvey register during the previous character time:

$$dHR06 = SFG\ HRIN + - - -$$

$$HRIN = W9\ HR00 + - - -$$

This code is shifted through the Harvey register again and encoded onto the tape a second time.

3-240 Escape from control state 2 is controlled by the buffer. When the last character is transmitted, W5 is left true as part of the halt interlock condition. In the normal write sequence, CUFF is set and the 9448 goes to CS3.

$$jCSC = CS2\ W5\ CUFF + - - -$$

$$CS3 = \overline{CSA}\ CSB\ CSC$$

When a file mark is written, CSRF gets set at the end of the first character time and the file mark flip-flop is turned on four bit-times later while the file mark character is repeating:

$$sCFMF = CS2\ W5\ CSRF\ WSA\ WCP1 + - - -$$

With CFMF set, the 9448 will enter CS3 even though CUFF was left reset:

$$jCSC = CS2\ W5\ CFMF + - - -$$

In either write sequence, normal or file mark, CECF is turned on to control the duration of CS3:

$$jCECF = CS2\ (CUFF + CFMF)\ WGO1 + - - -$$

$$cCECF = \underline{FC}$$

3-241 Write or Erase Forward (CS3)

3-242 In control state 3, the postamble code is written in a manner similar to that used for the preamble in CS1.

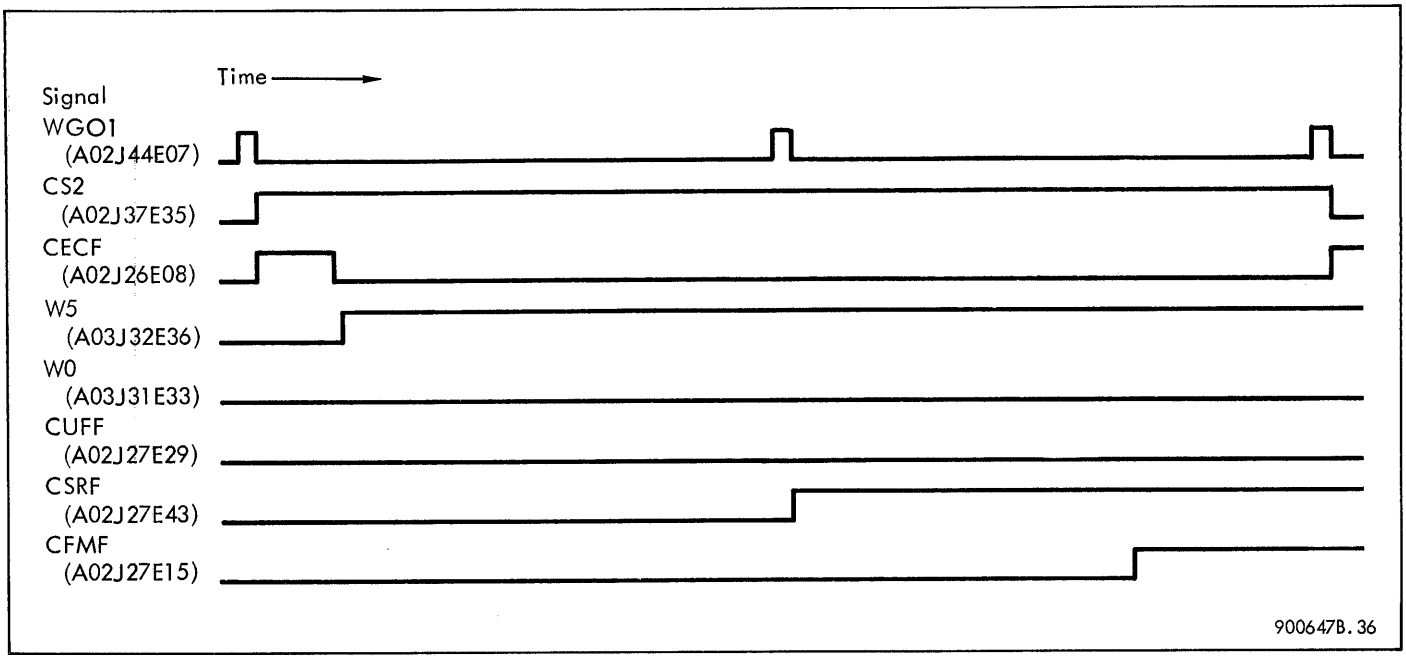


Figure 3-31. File Mark Write Sequence

Since CECF is on for the first character time, the postamble zero transition is encoded in WF as the first bit:

$$jWF = kWF = W9\ CSG$$

$$cWF = \underline{WCP1} + CS3\ CECF\ \overline{WSA}\ \overline{WSB}\ \overline{WSC}\ \underline{WCP0} + - - -$$

Afterwards, WF is clocked only by WCP1 producing the postamble ones. The external clock flip-flop gets turned off at the end of the first seven bit-times:

$$kCECF = CS13\ WGO1 + - - -$$

$$cCECF = \underline{FC}$$

$$CS13 = \overline{CSA}\ CSC$$

Two more bit-times of ones are recorded, and then the erase tape flip-flop is set to terminate the postamble code emitted on WFAS:

$$sCETF = CS3\ \overline{CECF}\ WSB\ WCP1 + - - -$$

$$WDAS = \overline{CETF}\ WF$$

If an erase operation is in progress, CETF was never turned off in CS1 and dc erasing is accomplished throughout CS1, CS2, and CS3.

3-243 With CECF reset, the 9448 is free to depart CS3 at the end of the character time. For a writing sequence, control state 4 is entered.

$$jCSA = CS3\ \overline{CECF} + - - -$$

$$kCSB = CS3\ \overline{CECF} + - - -$$

$$kCSC = CS3\ \overline{W10}\ \overline{CECF} + - - -$$

$$cCSA = cCSB = cCSC = \underline{WGO1}$$

Since the reset input to CSC is qualified for the non-erase condition, it will remain set as the 9448 departs CS3 in an erase sequence. The effect is to take the control state counter to CS5 instead of CS4:

$$CS4 = CSA\ \overline{CSB}\ \overline{CSC}$$

$$CS5 = CSA\ \overline{CSB}\ CSC$$

In either sequence, CECF is set as the 9448 leaves CS3 in order to provide clearing of the Harvey register in CS4 or CS5:

$$jCECF = CS13\ WGO1 + - - -$$

$$cCECF = \underline{FC}$$

$$CS13 = \overline{CSA}\ CSC$$

Incidentally, the continue flip-flop is reset in CS3 to permit a continue sequence in CS5:

$$rCUFF = CS13 + - - -$$

$$CS13 = \overline{CSA}\ CSC$$

3-244 Write or Erase Forward (CS4)

3-245 The read enable flip-flop is set in control state 1:

$$sCERF = CS13$$

$$CS13 = \overline{CSA}\ CSC$$

The read-after-write test is therefore started just before the writing of the preamble:

$$gRSF1 = gRSF2 = CERF$$

$$dRSF1 = RDAS\ \overline{TEST} + - - -$$

$$cRDA = cRDB = cRDC = cRDD = \underline{FC}$$

$$cRSA = cRSB = cRSC = \underline{RC} + RG\ \underline{FC}$$

$$rRSE = rRSF = (STRT + \overline{CERF}\ FC)\ dc$$

The distance between the write and read head is 0.3 inch, which corresponds to 60 characters or about 15 words at 4 characters per word. Accordingly, the read synchronizer will detect the preamble code while the 9448 is in CS2 if the record is longer than 15 words. When writing of the record is completed, the read synchronizer should not confirm the postamble until approximately 40 milliseconds have elapsed corresponding to the time required for the tape to traverse the interhead distance at 7.5 ips.

3-246 Control state 4 is inserted in the write sequence primarily to allow time for the record to traverse the interhead distance. When the read synchronizer detects gap, presumably in CS4 after confirming the postamble, CERF is reset:

$$rCERF = CSA\ \overline{CUFF}\ (RSF + - - -)\ RGFC + - - -$$

If a gap occurs after the preamble is detected, CERF is reset anyway:

$$rCERF = CSA\ \overline{CUFF}\ (RSD + - - -)\ RGFC + - - -$$

3-247 A premature gap does produce an error signal to the buffer:

$$RES = RG\ RSD\ FC + - - -$$

$$\overline{Wes} = \overline{RES + - - -}$$

but a premature stopping sequence as a result of the early gap would be very dangerous to previous records if it were followed by an erase reverse operation. Accordingly, CS4 is timed out to 34.7 milliseconds, or about 10% less than the expected interhead tape motion time, before the gap is honored. This is the write-to-read delay, WTRD, produced in the Harvey register:

$$WTRD = HR05\ HR04\ HR01\ HR00\ WGO1$$

WTRD can be true at many counts after the 34.7-millisecond point is reached. The Harvey register is reset to zero by CECF which was set in CS3 or CS7:

$$cHR00 = \underline{SPP} + - - -$$

$$\vdots$$

$$cHR06 = \underline{SPP} + - - -$$

$$SPP = \overline{CS0}\ \overline{CS7}\ CECF\ \underline{FC}$$

(All repeater input gates are false at this time, so the register is clocked to zero.)

3-248 After one-half of a bit-time interval, CECF is reset:

$$kCECF = (CS4 + - - -)\ WCP1$$

$$cCECF = \underline{FC}$$

The Harvey register converts to a binary counter clocked by WGO1:

$$CBG = (CS4 + - - -)\ \overline{CECF} + - - -$$

When the WTRD count is reached, the control state counter can proceed to CS5 as soon as CERF is reset by the gap:

$$jCSC = CS4\ W9\ \overline{W10}\ \overline{CERF}\ WTRD + - - -$$

$$cCSC = \underline{WGO1}$$

$$CS5 = CSA\ \overline{CSB}\ CSC$$

Control state 5 will be entered as WTRD occurs if the gap occurred early.

3-249 Another condition could exist; namely, the gap is not detected. This will happen if erasure is not completed or no information is recorded because of dirt under the write head. The 9448 stays in CS4 waiting for CERF to reset, but only for a total of 50.7 milliseconds. This time interval, called the interhead guard delay, is recognized in the Harvey register:

$$IHGD = HR06\ HR03\ HR01\ HR00\ WGO1$$

Thus, about 25% additional time is allowed beyond the nominal interhead motion time after which the control state counter escapes to CS5:

$$jCSC = CS4\ \overline{W10}\ IHGD + - - -$$

$$cCSC = \underline{WGO1}$$

$$CS5 = CSA\ \overline{CSB}\ CSC$$

An overdue gap error signal is sent to the buffer

$$\overline{Wes} = \overline{RES + \overline{SELS}\ WES9}$$

$$Res = CS4\ \overline{W10}\ IHGD + - - -$$

In any case, CECF is set in order to provide clearing of the Harvey register in CS5:

$$\text{¡CECF} = \text{CS4}\ \overline{\text{CERF}}\ \text{WTRD}\ \overline{\text{W9 W10 C12M SELS}} + \text{CS4 IHGD} + - - -$$

$$\text{cCECF} = \underline{\text{FC}}$$

3-250 Write or Erase Forward (CS5)

3-251 Control state 5 provides the necessary delay to erase the last part of the 0.75-inch gap. In CS0, 0.225 inch of gap is generated. The interhead distance of 0.3 inch is erased in CS4. That leaves 0.225 inch of tape to be erased in the stopping sequence. The stop distance is approximately 0.03 inch, so CS5 lets the tape run at 7.5 ips for 0.195 inch before the stop command is given. The required time interval is 26.0 milliseconds, and is called the stop gap delay:

$$\text{SPGD} = \text{HR05 HR02 HR01 WGO1}$$

The Harvey register is reset to zero by CECF which was set in CS4 or CS7:

$$\text{cHR00} = \underline{\text{SPP}} + - - -$$
$$\vdots$$
$$\text{cHR06} = \underline{\text{SPP}} + - - -$$

$$\text{SPP} = \overline{\text{CS0}}\ \overline{\text{CS7}}\ \text{CECF}\ \underline{\text{FC}}$$

(All repeater input gates are false at this time, so the register is clocked to zero.)

3-252 After one-half of a bit time interval, CECF is reset:

$$\text{kCECF} = (\text{CS5} + - - -)\ \text{WCP1} + - - -$$

$$\text{cCECF} = \underline{\text{FC}}$$

The Harvey register converts to a binary counter clocked by WGO1 (1.5 kc):

$$\text{CBG} = (\text{CS56} + - - -)\ \overline{\text{CECF}}$$

$$\text{CS56} = \text{CS5} + - - -$$

When the SPGD count is reached, the control state counter can proceed to CS6 if a continue command is not received:

$$\text{¡CSB} = \text{CS5 SPGD}\ \overline{\text{CUFF}} + - - -$$

$$\text{kCSC} = \text{CS5 SPGD}\ \overline{\text{CUFF}} + - - -$$

$$\text{cCSB} = \text{cCSC} = \underline{\text{WGO1}}$$

$$\text{CS6} = \text{CSA CSB}\ \overline{\text{CSC}}$$

3-253 In CS5 (before SPGD), if the computer program tests for gap (SKS12610), an affirmative reply will be given:

$$\overline{\text{Sio}} = \overline{\text{C12}}\ \text{C13}\ \overline{\text{C14}}\ \text{C15 C16 CS5}\ \overline{\text{CUFF}}\ \overline{\text{CFMF}} + - - -$$

A new start command may be given which calls for continuation of tape motion without stopping. A start command in CS5 will set the continue flip-flop:

$$\text{sCUFF} = \text{CS5 STRT} + - - -$$

The stop gap delay is ignored by the logic if CUFF is on. Instead the Harvey register continues to count, providing a time interval corresponding to 0.75 inch of tape travel at 7.5 ips less the interhead distance already traveled in CS4. The required delay is 60.7 milliseconds and is called the continue write delay:

$$\text{CUWD} = \text{HR06 HR04 HR03 HR01 WGO1}$$

At the CUWD count, the control state counter goes back to control state 1 to write the preamble for the next record:

$$\text{kCSA} = \text{CS5 W9 CUFF CUWD}$$

$$\text{cCSA} = \underline{\text{WGO1}}$$

$$\text{CS1} = \overline{\text{CSA}}\ \overline{\text{CSB}}\ \text{CSC}$$

The external clock flip-flop must be set to prepare for its roll in controlling the duration of CS1:

$$\text{¡CECF} = \text{CS5 W9 CUFF CUWD} + - - -$$

3-254 Write or Erase Forward (CS6)

3-255 In the absence of the continue command, the control state counter goes from CS5 to CS6 when the stop gap delay has been timed out. In control state 6, the STOP command line is made true to the tape transport unit electronics:

$$\text{STOP} = \overline{\text{HR05}}\ \text{CS6} + - - -$$

The Harvey register is reset to zero by CECF, which was set in CS5 for write or erase forward sequences:

$$\text{cHR00} = \underline{\text{SPP}} + - - -$$
$$\vdots$$
$$\text{cHR06} = \underline{\text{SPP}} + - - -$$

$$\text{SPP} = \overline{\text{CS0}}\ \overline{\text{CS7}}\ \text{CECF}\ \underline{\text{FC}}$$

(All repeater input gates are false at this time, so the register is clocked to zero.)

After one-half of a bit time interval, CECF is reset:

$$\text{kCECF} = (\text{CS6} + - - -)\ \text{WCP1} + - - -$$

$$\text{cCECF} = \underline{\text{FC}}$$

The Harvey register converts to a counter clocked by WGO1 (1.5 kc):

$$CBG = (CS56 + - - -)\ \overline{CECF} + - - -$$

$$CS56 = CS6 + - - -$$

3-256 With the STOP line true, the forward pressure roller disengages and the tape comes to a stop. When the Harvey register has counted to 32, HR05 is turned on, removing the STOP signal. The duration of the STOP signal is thus established at 21.3 milliseconds, which allows ample time to stop the tape. At the fall of the STOP signal, the transport deselects, making the SELS bus go false. The write tape signal is dropped, removing write current:

$$WRTS = W9\ SELS$$

The Harvey register continues to count until the stop tape delay is recognized 9.0 milliseconds later:

$$SPTD = HR05\ HR03\ HR02\ HR00\ WGO1$$

At this time the skip remainder flip-flop gets set:

$$sCSRF = CS6\ SPTD + - - -$$

The halt signal is sent to the buffer:

$$Whs = \overline{CS6\ CSRF + - - -}$$

When the buffer resets its address lines in response to the halt signal, the control state counter returns to CS0:

$$rCSA = rCSB = (\overline{W11}\ \overline{STRT})\ dc$$

$$CS0 = \overline{CSA}\ \overline{CSB}\ \overline{CSC}$$

3-257 Read or Scan Forward (CS0)

3-258 In the stopped condition, the beginning of the next record is 0.525 inch from the read head. In order to avoid spurious information that might be in the gap, the read logic is not enabled until 50.7 milliseconds after the STRT command is executed (see figure 3-32). The delay is accomplished by holding the 9448 in control state 0 until the Harvey register has counted to the code recognized as the interhead guard delay:

$$IHGD = HR06\ HR03\ HR01\ HR00\ WGO1$$

After the 50.7 milliseconds have elapsed, the control state counter goes directly into CS7 from CS0:

$$jCSA = CS0\ IHGD + - - -$$

$$jCSB = CS0\ IHGD + - - -$$

$$jCSC = CS0\ IHGD + - - -$$

$$cCSA = cCSB = cCSC = \underline{WGO1}$$

$$CS7 = CSA\ CSB\ CSC$$

Since CUFF is held set before the buffer selects tape unit operations, its output will be true as the 9448 departs CS0:

$$sCUFF = \overline{W11} + - - -$$

The external clock flip-flop is reset at the end of CS0 in read or scan forward operations:

$$kCECF = CS0\ IHGD + - - -$$

$$cCECF = \underline{FC}$$

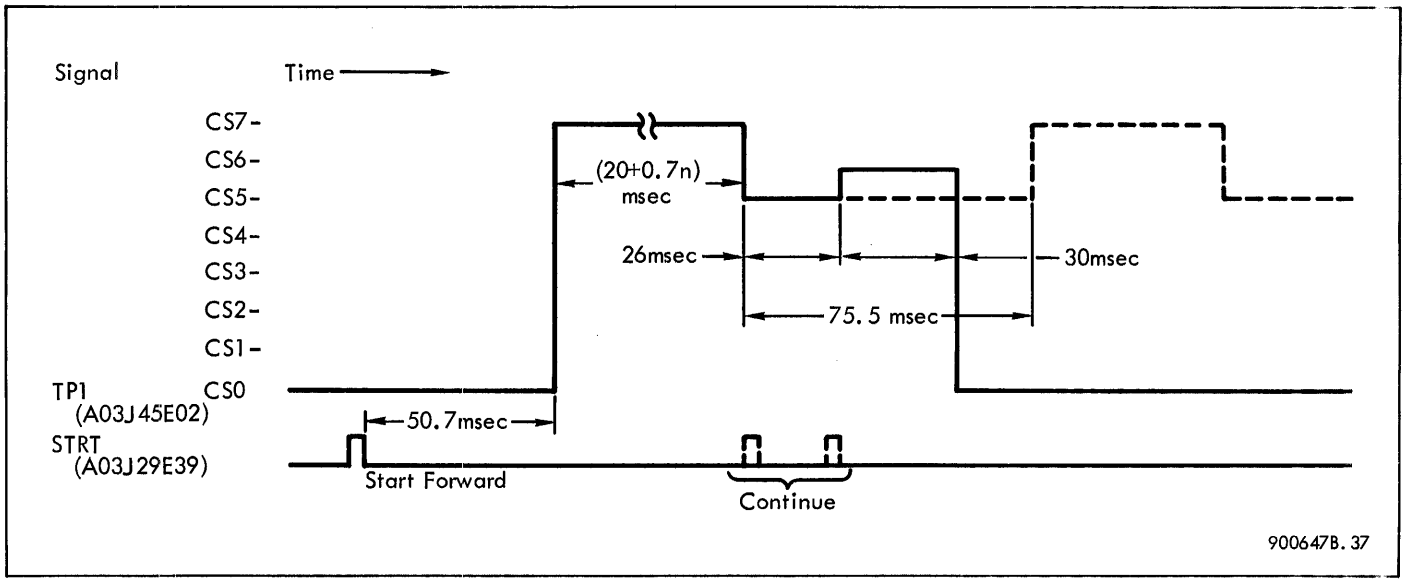


Figure 3-32. Read/Scan Forward Control State Sequence

3-259 Read or Scan Forward (CS7)

3-260 The actual reading of a record is performed in control state 7. The read enable flip-flop is set by CUFF, which was left true in CS0 and made true in CS5 for continued operations:

sCERF = CS7 CUFF + - - -

The file mark flip-flop is also armed at the beginning of CS7:

sCFMF = CS7 CUFF + - - -

After performing the job of setting CERF and CFMF at the beginning of CS7, CUFF is reset:

rCUFF = CS7 WCP1 + - - -

With CERF set, the read decoder can supply bits through RF into the read synchronizer, which in turn detects the preamble:

jRSD = $\overline{RF}$ RSA RSB $\overline{RSF}$ $\overline{RG}$

cRSD = RC + - - -

3-261 The read flip-flop is also connected to the Harvey register:

HRIN = $\overline{W9}$ RF + - - -

which shifts forward clocked by RC:

dHR00 = SFG HR01 + - - -
⋮
dHR05 = SFG HR06 + - - -

dHR06 = SFG HRIN + - - -

cHR00 = SSP + - - -
⋮
cHR06 = SSP + - - -

SFG = CS27 $\overline{C12M}$ $\overline{CECF}$

CS27 = CS7 + - - -

SSP = CS7 RC + - - -

With RSD set, the read synchronizer counts through 7-bit cycles and produces the read character pulse:

RCP = RSA RSB RSD ($\overline{RSF}$ + $\overline{RF}$) RC

The external clock flip-flop is set as the seventh bit of each character is shifted into the Harvey register:

jCECF = CS7 RCP + - - -

cCECF = FC

This clocks the buffer:

$\overline{Ecw}$ = $\overline{CS27\ CERF\ \overline{CSRF}\ CECF}$ + - - -

CS27 = CS7 + - - -

The contents of the Harvey register are transferred in parallel to the buffer:

$\overline{Zw1}$ = $\overline{CS7\ HR01}$
⋮
$\overline{Zw6}$ = $\overline{CS7\ HR06}$

$\overline{Zwp}$ = $\overline{CS7\ HR00}$

When W6 is made true in the buffer, the external clock flip-flop is reset:

kCECF = CS27 W6 + - - -

cCECF = FC

CS27 = CS7 + - - -

3-262 If a non-file mark code is present in the Harvey register at the time a character is transferred to the buffer, the file mark flip-flop is reset:

rCFMF = CS7 W5 W6 $\overline{FMCD}$ + - - -

FMCD = HR00 $\overline{HR01}$ $\overline{HR02}$ HR03 HR04 HR05 HR06

A gap in the record also will prevent a file mark from being detected:

rCFMF = RSD RG FC + - - -

If a true file mark is present, CFMF will remain set through the end of the record. The file mark flip-flop may be tested by the program using the SKS13610 instruction:

$\overline{Sio}$ = $\overline{C12}$ C13 C14 C15 C16 CUG CFMF + - - -

3-263 Characters continue to be transferred to the buffer until the end of the record unless the program executes an EOM13610 to skip the remainder of the record. The skip remainder flip-flop is set by this instruction:

sCSRF = CS7 CNTL ($\overline{C12}$ C13 C14 C15 C16) + - - -

CNTL = Ioc $\overline{C17}$ C20

The buffer may receive no more clocks:

$\overline{Ecw}$ = $\overline{CS27\ CERF\ \overline{CSRF}\ CECF}$ + - - -

Whenever the gap is detected, the read enable flip-flop is turned off:

$$rCERF = CSA\ \overline{CUFF}\ (RSD + RSF)\ RG\ FC + - - -$$

This also inhibits clocks to the buffer and permits the control state counter to escape from CS7. In read or scan forward operations, the 9448 goes to CS5:

$$kCSB = CS7\ \overline{CERF} + - - -$$

$$cCSB = \underline{WGO1}$$

$$CS5 = CSA\ \overline{CSB}\ CSC$$

The external clock flip-flop is set at the end of CS7 for clearing the Harvey register in CS5:

$$jCECF = CS7\ \overline{CERF}\ WGO1 + - - -$$

$$cCECF = \underline{FC}$$

3-264 Read or Scan Forward (CS5, CS6)

3-265 The purpose of control state 5 in read or scan forward operations is the same as in write or erase forward operations except that erasing is not performed, of course. The stop gap delay generated by the Harvey register lets the tape move to a position such that when the STOP command is given in CS6, the tape will stop with the heads symmetrically stationed in the gap. As described in paragraph 3-253, the presence of the gap may be tested by the program and a continue command may be given during the 26.0 milliseconds before SPGD. If the program executes an EOM0361n, EOM0261n, EOM0363n, or EOM0263n, the read sequence is to be continued. The continue flip-flop is set:

$$sCUFF = CS5\ \ STRT + - - -$$

3-266 With CUFF in the one state, the control logic ignores the SPGD signal, and the Harvey register continues counting for a total of 75.5 milliseconds. This represents a time about 25% less than that required to traverse the full 0.75 inch of the gap, and spurious bits in the gap are thereby ignored. At the end of the 75.5 milliseconds, the Harvey register detects the continue read delay code:

$$CURD = HR06\ HR05\ HR04\ HR03\ WGO1$$

The control state counter goes back to CS7 to permit reading of the next record:

$$jCSB = CS5\ \ CUFF\ \ CURD + - - -$$

$$cCSB = \underline{WGO1}$$

$$CS7 = CSA\ \ CSB\ \ CSC$$

3-267 In the absence of a continue command before SPGD time, the control state counter goes to CS6 which issues the STOP command to the transport:

$$jCSB = CS5\ SPGD\ \overline{CUFF} + - - -$$

$$kCSC = CS5\ SPGD\ \overline{CUFF} + - - -$$

$$cCSB = cCSC = \underline{WGO1}$$

$$CS6 = CSA\ \ CSB\ \ \overline{CSC}$$

$$STOP = \overline{HR05}\ \ CS6 + - - -$$

Throughout CS5 and CS6, the magnetic tape gap signal is given to unlock the buffer if it is in the scan condition:

$$\overline{(Mtg)} = CS56\ \overline{CUFF} + - - -$$

$$CS56 = CS5 + CS6$$

3-268 Scan Reverse (CS0, CS7, CS4, CS5, CS6)

3-269 Scan reverse is accomplished in a somewhat different sequence from that used in read or scan forward operations. Only the differences will be described here.

3-270 Since the read head precedes the write head in reverse operations, control state 0 is made only 0.7 millisecond long (see figure 3-33). Accordingly, entrance into CS7 occurs after only one character time in CS0:

$$jCSA = CS0\ \overline{W9}\ C12M + - - -$$

$$jCSB = CS0\ \overline{W9}\ C12M + - - -$$

$$jCSC = CS0\ \overline{W9}\ C12M + - - -$$

$$cCSA = cCSB = cCSC = \underline{WGO1}$$

$$CS7 = CSA\ \ CSB\ \ CSC$$

3-271 The read synchronizer detects the postamble in reverse as if it were a preamble. The Harvey register is clocked by RC and shifts reverse accepting the output of RF into HR00:

$$dHR00 = SRG\ \ RF + - - -$$

$$dHR01 = SRG\ \ HR00 + - - -$$

$$\vdots$$

$$dHR06 = SRG\ \ HR05 + - - -$$

$$cHR00 = \underline{SSP} + - - -$$

$$\vdots$$

$$cHR06 = \underline{SSP} + - - -$$

$$SRG = CS27\ C12M\ \overline{CECF}$$

$$SSP = CS7\ \underline{RC} + - - -$$

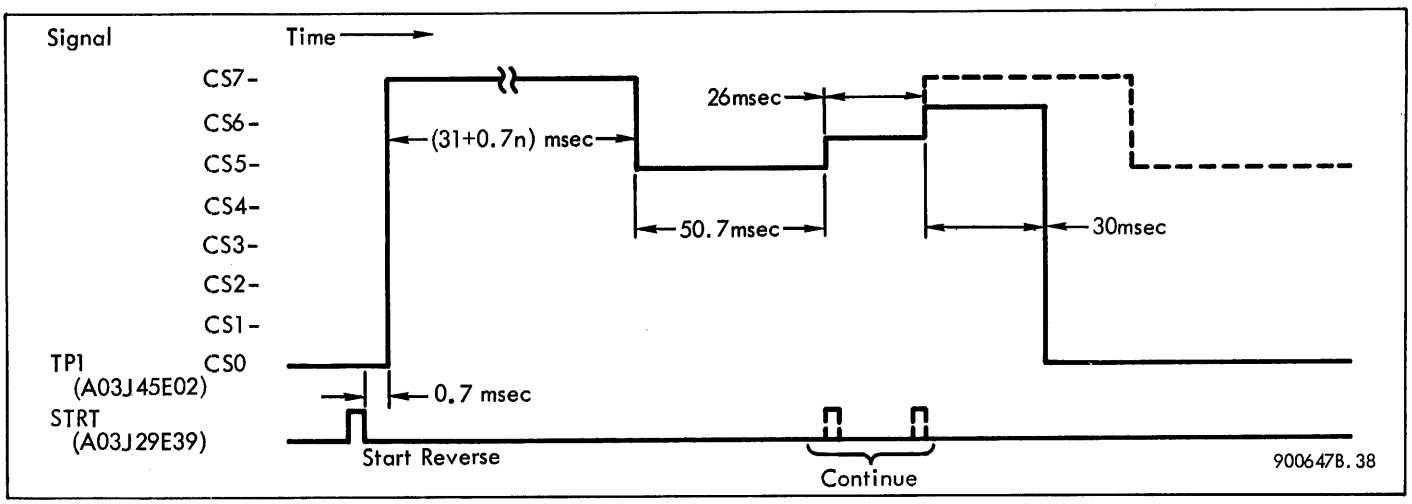


Figure 3-33. Scan Reverse Control State Sequence

Characters transfer to the buffer clocked by CECF as described in paragraph 3-261. The preamble is detected in reverse as if it were the postamble, and CERF is reset at the end of the record:

$$rCERF = CSA\ \overline{CUFF}\ (RSD + RSF)\ RG\ FC + - - -$$

3-272 The control state counter goes into CS4 in reverse to provide additional delay so that the tape can be stopped with the write head in front of the record just scanned:

$$kCSB = CS7\ \overline{CERF} + - - -$$

$$kCSC = CS7\ C12M\ \overline{CERF} + - - -$$

$$cCSB = cCSC = \underline{WGO1}$$

$$CS4 = CSA\ \overline{CSB}\ \overline{CSC}$$

3-273 The Harvey register gets cleared to zero in CS4 because CECF is set as the 9448 departs CS7:

$$jCECF = CS7\ \overline{CERF}\ WGO1$$

$$cCECF = \underline{FC}$$

Counting takes place in the Harvey register in CS4 as described in paragraph 3.243. When the write-to-read delay (34.7 milliseconds) has elapsed, the control state counter goes into CS5:

$$jCSC = CS4\ \overline{W9}\ WTRD + - - -$$

$$cCSC = \underline{WGO1}$$

$$CS5 = CSA\ \overline{CSB}\ CSC$$

The scan reverse sequence from here on is the same as for read or scan forward, as described under paragraph 3.255.

3-274 Erase Reverse (CS0, CS1, CS2, CS3, CS4, CS6)

3-275 In an erase reverse operation, the 9448 follows a sequence only slightly different from that described in paragraphs 3-231 through 3-256. An important difference occurs in CS1. First, it should be noted that accumulated mechanical tolerances can produce substantial differences between starting and stopping distances in the forward and reverse directions. A long forward stop distance in conjunction with a short reverse stop distance could leave a portion of the record unerased. This situation is aggravated by a long forward start distance as the program attempts to rewrite the record. On the other hand, if the forward stop distance is short and the reverse stop distance is long, the tape could back up too far. A short gap would result in the rewrite process, a condition further aggravated by a short forward start distance. More significant than this, however, is the fact that repeated cycles of writing forward and erasing reverse would place the preceding record in danger of partial erasure.

3-276 The desired effect, therefore, is to have the tape stop in the reverse direction with the write head farther away from the preceding record than it was when that record was written, but still in front of the faulty record to guarantee its complete erasure. The net tape movement would allow the program to produce a forward "creep" over the presumably bad spot on the tape.

3-277 After the start gap delay generated in CS0, the tape should be moved backwards to a position where the read is just encountering the previously written record. The control state counter goes into CS1:

$$jCSC = CS0\ W9\ STGD + - - -$$

$$cCSC = \underline{WGO1}$$

$$CS1 = \overline{CSA}\ \overline{CSB}\ CSC$$

The enable read flip-flop is set in CS1:

$$sCERF = CS13 + - - -$$

$$CS13 = \overline{CSA}\ CSC$$

The external clock flip-flop will reset after the first character time has elapsed:

$$kCECF = CS13\ WGO1 + - - -$$

$$cCECF = \underline{FC}$$

3-278 If the record is being read, the read gap signal will be false, but if the read head has not yet reached the record, the read decoder will make RG true. This will set CECF true again in control state 1:

$$sCECF = CS1\ W10\ C12M\ RG + - - -$$

3-279 The control state counter will be stalled in CS1 (see figure 3-34). After seven bit times have elapsed, CECF is reset again by WGO1. During the subsequent character time CECF can be set again by RG, but if seven "gap-free" bits appear, CECF will be left reset and the control state counter can proceed to CS2.

$$jCSB = CS1\ \overline{CECF} + - - -$$

$$kCSC = CS1\ \overline{CECF} + - - -$$

$$cCSB = cCSC = \underline{WGO1}$$

$$CS2 = \overline{CSA}\ CSB\ \overline{CSC}$$

3-280 The timing of CS2 is controlled by the number of characters outputted by the computer, the logic of which is described under paragraph 3-235. When the halt interlock is manifested by the buffer, the 9448 enters CS3 for two character times as described under paragraph 3-241.

At the end of CS3, the read head is positioned just in front of the record. The control state counter proceeds to CS4:

$$jCSA = CS3\ \overline{CECF} + - - -$$

$$kCSB = CS3\ \overline{CECF} + - - -$$

$$kCSC = CS3\ C12M\ \overline{CECF} + - - -$$

$$cCSA = cCSB = cCSC = \underline{WGO1}$$

3-281 The Harvey register gets cleared to zero by CECF in CS4 as described in paragraph 3-247. It then converts to a counter, and meters out a tape distance amounting to approximately 25% more than the nominal interhead distance. The interhead guard delay is recognized after 50.7 milliseconds have elapsed:

$$IHGD = HR06\ HR03\ HR01\ HR00\ WGO1$$

At this time the tape record has moved backwards beyond the write head and has been safely erased.

3-282 The control state counter skips CS5 because no more delay is called for in erase reverse. This means that the continue option is defeated for erase reverse. When the IHGD is recognized, the 9448 goes directly from CS4 to CS6:

$$jCSB = CS4\ W10\ IHGD + - - -$$

$$cCSB = \underline{WGO1}$$

$$CS6 = CSA\ CSB\ \overline{CSC}$$

The external clock flip-flop is set to clear the Harvey register in CS6:

$$jCECF = CS4\ IHGD + - - -$$

$$cCECF = \underline{FC}$$

The STOP command is issued to the transport in CS6 as described in paragraph 3-255.

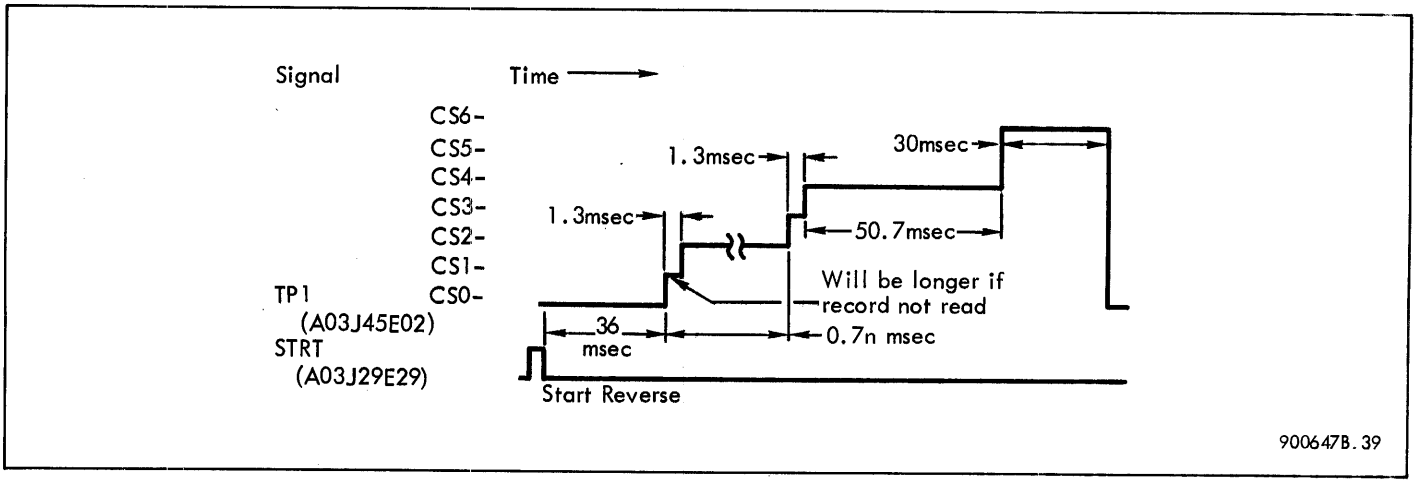


Figure 3-34. Erase Reverse Control State Sequence

3-283 The functions performed by the tape control unit in each control state are summarized in figure 3-35 and tables 3-4 and 3-5.

3-284 REWINDING

3-285 The rewind function is performed by MAGPAK as an off-line operation. The rewind instruction, EOM1401n, is decoded and relayed to the tape transport unit electronics.

$$REWM = CNTL\ C12\ \overline{C16}\ \overline{TEST}$$

$$CNTL = Ioc\ \overline{C17}\ C20$$

The least significant three bits in the C-register are continuously decoded as logical tape unit addresses:

$$LLT0 = \overline{C21}\ \overline{C22}\ \overline{C23}$$

$$\vdots$$

$$LLT7 = C21\ C22\ C23$$

The UNIT SELECT switch on the 9446 determines which transport will honor the rewind command.

3-286 AUXILIARY CONTROL LOGIC

3-287 If a conventional magnetic tape system, such as SDS Model 9246/9248, is required to operate over the same computer input-output channel as the MAGPAK, the 9248 control unit is cabled into the 9448 MAGPAK control unit. Particularly, P40 replaces the dummy cable-plug module in location A03J41.

3-288 Compatibility and noninterference is ensured by the UNIT SELECT switches on the 9246 and 9446 manual control panels. The external clock, buffer halt signal, gap signal, and error signal from the 9248 are forwarded to the computer buffer via the following logic:

$$\overline{Ecw} = \overline{ECM9 + - - -}$$

$$\overline{Whs} = \overline{WHS9 + - - -}$$

$$Mtg = MTG9 + - - -$$

$$\overline{Wes} = \overline{\overline{SELS}\ WES9 + - - -}$$

3-289 The control unit gate (CUG) participates in the auxiliary logic in several ways. To understand this term it is first necessary to observe that CSRF is left set after performing its function of halting the buffer:

$$sCSRF = CS6\ SPTD + - - -$$

$$\overline{Whs} = \overline{CS6\ CSRF + - - -}$$

The control unit gate is developed as follows:

$$CUG = CSA + CSB + CSC + CECF + CSRF$$

and is therefore true whenever the MAGPAK control unit is selected for operation, and it is also held true by CSRF after MAGPAK has completed the operation. The file mark flip-flop in the 9448 may be tested by an SKS13610 after a MAGPAK operation:

$$\overline{Sio} = \overline{C12}\ C13\ C14\ C15\ C16$$

$$CUG\ CFMF + - - -$$

3-290 If a command is given to the 9248, it is necessary to turn off the control unit gate. This condition is detected if a SELS signal has not appeared before Q2 falls. Thus, CSRF is reset turning off CUG if any STRT command does not result in the selection of a MAGPAK transport:

$$rCSRF = STRT\ \overline{Q2}\ \overline{SELS} + - - -$$

$$CUG = CSRF + - - -$$

Tests for end-of-file will come from the 9248 with CUG at zero:

$$\overline{Sio} = \overline{\overline{C12}\ C13\ C14\ C15\ C16\ CUG}\ \overline{SI09 + - - -}$$

$$= \overline{(\overline{C12}\ C13\ C14\ C15\ C16 + \overline{CUG})\ \overline{SI09} + - - -}$$

3-291 The 9448 is arranged to tamper with certain control logic signals coming from the computer that are used in the 9248. First $\overline{C17}$ and C20 are made true permanently at the auxiliary connector (A03J41):

$$\overline{C179} = 1$$

$$C209 = 1$$

The Buc signal forwarded to the 9248 is qualified properly so that only magnetic tape commands can be honored in the 9248:

$$BUC9 = STRT + CS7$$

$$STRT = BUC\ \overline{C17}\ C20$$

The control state 7 term above has the effect of locking out 9248 inputs on the Z lines when MAGPAK is reading.

3-292 Rewind and skip-remainder commands are also properly qualified inasmuch as the Ioc line to the 9248 is provided the following logic:

$$IOC9 = CNTL$$

$$CNTL = IOC\ \overline{C17}\ C20$$

The computer clock to the 9248 is blocked by CUG when MAGPAK is in operation:

$$Q29 = Q2 + CUG$$

W9 = WRITE
$\overline{W9}$ = READ

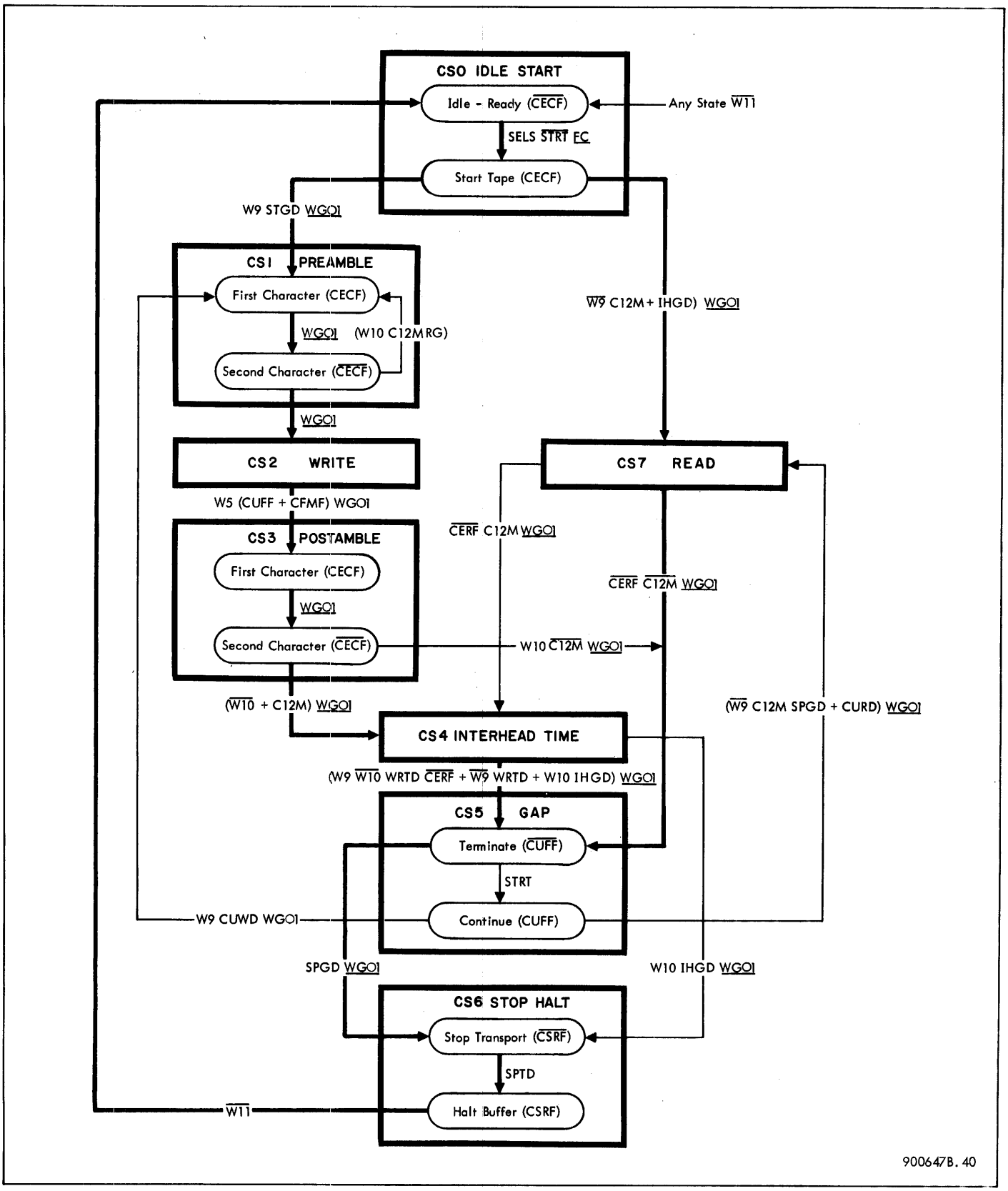


Figure 3-35. MAGPAK Control Logic State Diagram

Table 3-4. Model 9448 Tape Control Logic

Control State	Logical Conditions	Time	Action	Explanation
CS0:				
$\overline{CSA}\ \overline{CSB}\ \overline{CSC}$	$\overline{W11}$		0 ⟶ CECF	Idle-Ready Condition:
			0 ⟶ (CSA-CSC)	Hold Control State CS0
	PREVIOUS CONDITIONS		0 ⟶ (WCA-WCD)	Cage Write Clock Generator
			0 ⟶ (WSA-WSC)	Cage Write Synchronizer
			0 ⟶ CERF	Disable Read
			0 ⟶ CETF	Disable Erase
			0 ⟶ C12M	Clear Reverse Monitor
			1 ⟶ CUFF	Arm Continue FF for CS7
	CSRF		CUG = 1	Cage 9248 on Auxiliary Connector
	$\overline{C17}$ C20 $\overline{Q2}$ $\overline{SELS}$	BUC	0 ⟶ CSRF	Uncage 9248 on Auxiliary Connector
	$\overline{C17}$ C20 $\overline{C12}$	BUC	T12S = 1	Command Addressed Tape Forward
	$\overline{C17}$ C20 C12	BUC	S12T = 1	Command Addressed Tape Reverse
			1 ⟶ C12M	Set Reverse Monitor FF
	W11 $\overline{BUC}$ SELS	FC	1 ⟶ CECF	Tape Selected, End Idle-Ready, Arm Character Count for CS1
	CECF	FC	(WCA-WCD) + 1	Write Clock Generator Counts
		WCP0	(WSA-WSC) + 1	Write Synchronizer Counts
		WCP1	0 ⟶ CSRF	Clear Auxiliary Lock-Out
	W9 W11 WCP1		1 ⟶ CETF	Enable Erase
	$\overline{W9}$ C12M	WGO1	0 ⟶ CECF	Scan Reverse: Reset Clock for CS7
			1 ⟶ CSA	Scan Reverse: ⟶ CS7
			1 ⟶ CSB	
			1 ⟶ CSC	
		WGO1	(HR) + 1	Harvey Register Counts
	W9 STGD	WGO1	1 ⟶ CSC	Write: Start Gap Delay ⟶ CS1
	IHGD	WGO1	0 ⟶ CECF	Read/Scan Forward: Reset Clock for CS7
			1 ⟶ CSA	Read/Scan Forward: Interhead Guard Delay ⟶ CS7
			1 ⟶ CSB	
			1 ⟶ CSC	

Table 3-4. Model 9448 Tape Control Logic (Cont.)

Control State	Logical Conditions	Time	Action	Explanation
CS1: $\overline{CSA}$ $\overline{CSB}$ CSC	$\overline{W10}$ WSA WSC	WCP1	0 ⟶ CETF	Write: Disable Erase after 5 Bit Times
			1 ⟶ CERF	Write: Enable Read
		WGO1	0 ⟶ CECF	End of First Character Time
	$\overline{CECF}$ WSA WSB	WCP1	$\overline{WF}$ ⟶ WF	Write 8 Ones in Preamble
		WCP0	$\overline{WF}$ ⟶ WF	Write Zero for End of Preamble
	CECF		0 ⟶ (HR)	Clear Harvey Register for CS2
		WCP1	0 ⟶ CUFF	Initialize File Mark Duplication Logic for CS2
			0 ⟶ CSRF 0 ⟶ CFMF	
	W10 C12M RG	FC	1 ⟶ CECF	Erase Reverse: Stall to Record
	$\overline{CECF}$	WGO1	1 ⟶ CSB	Write/Erase: ⟶ CS2
			0 ⟶ CSC	
			1 ⟶ CECF	Write/Erase: Provide First Buffer Clock For CS2
CS2: $\overline{CSA}$ CSB $\overline{CSC}$	$\overline{W5}$ $\overline{CSRF}$ CECF		ECM = 1	External Clock to Buffer
	W6	FC	0 ⟶ CECF	Reset Buffer Clock
	CECF	FC	(R) ⟶ (HR)	Output Character to Harvey Register
	$\overline{HR00}$	WCP0	$\overline{WF}$ ⟶ WF	Write Contents of Harvey Register
		WCP0	(HR) Forward	Recirculate Harvey Register Forward
	$\overline{SELS}$		WHS = 1	Tape Deselect (BOT): Halt Buffer
	W0 WSB	WCP1	1 ⟶ CUFF	Normal Write Sequence
	$\overline{CUFF}$	WGO1	1 ⟶ CSRF	File Mark Write Sequence: Delay to Repeat Character
	W5 CSRF WSA	WCP1	1 ⟶ CFMF	
	CUFF + CFMF	WGO1	1 ⟶ CECF	Write/Erase: Clock to Buffer or Arm Character Count for CS3
	W5 (CUFF + CFMF)	WGO1	1 ⟶ CSC	Write/Erase: Halt Interlock ⟶ CS3

Table 3-4. Model 9448 Tape Control Logic (Cont.)

Control State	Logical Conditions	Time	Action	Explanation
CS3: $\overline{CSA}$ CSB CSC	CECF $\overline{WSA}$ $\overline{WSB}$ $\overline{WSC}$	WCP0	$\overline{WF}$ → WF	Write Zero for Beginning of Postamble
		WCP1	$\overline{WF}$ → WF	Write 8 Ones in Postamble
		WGO1	0 → CECF	End of First Character Time
	$\overline{CECF}$ WSB	WCP1	1 → CETF	Enable Erase After 2 Bit-Times
		WCP1	0 → CUFF	Clear Continue and File Mark Detect Flip-Flops
			0 → (HR)	
	CECF		0 → (HR)	Clear Harvey Register for CS4
	W10 $\overline{C12M}$ $\overline{CECF}$	WGO1	1 → CSA	Erase Forward: → CS5
			0 → CSB	
	($\overline{W10}$ + C12M) $\overline{CECF}$	WGO1	1 → CSA	Erase Reverse/Write: → CS4
			0 → CSB	
			0 → CSC	
CS4: CSA $\overline{CSB}$ $\overline{CSC}$	CECF	FC	0 → (HR)	Scan Reverse: Clear Harvey Register
		WCP1	0 → CECF	Reset HR Clear Terminal
	$\overline{CECF}$	WGO1	(HR) + 1	Harvey Register Counts
	W9 $\overline{W10}$ $\overline{CERF}$ WTRD	WGO1	1 → CSC	Write: Gap → CS5
	$\overline{W10}$ IHGD	WGO1	1 → CSC	Write: No Gap Escape → CS5
	RSA RSB C12M	FC	1 → CECF	Reverse: No Gap; Clear HR
	$\overline{W9}$ WTRD	WGO1	1 → CSC	Scan Reverse: Interhead Delay → CS5
	$\overline{CUFF}$ (RSD + RSF) RG		0 → CERF	Detect Gap: Disable Read
	W10 IHGD	WGO1	1 → CSB	Erase Reverse: → CS6
	$\overline{CERF}$ WTRD + IHGD	WGO1	1 → CECF	Arm Clearing of Harvey Register in CS5 or CS6
CS5: CSA $\overline{CSB}$ CSC	CECF	FC	0 → (HR)	Clear Harvey Register
		WCP1	0 → CECF	Reset HR Clear Terminal
	$\overline{CECF}$	WGO1	(HR) + 1	Harvey Register Counts
	$\overline{CUFF}$		MTG = 1	Gap Signal to Buffer
			SKS TGT	Tape Gap Test Indicates Gap
	$\overline{C17}$ C20	BUC	1 → CUFF	Continue Command
		WCP1	0 → CSRF	Disable Buffer-Halt Terminal

Table 3-4. Model 9448 Tape Control Logic (Cont.)

Control State	Logical Conditions	Time	Action	Explanation
CS5: CSA $\overline{CSB}$ CSC (Cont.)	$\overline{CUFF}$ SPGD	WGO1	1 ⟶ CSB	No Continue: Stop Gap Delay ⟶ CS6
			0 ⟶ CSC	
	W9 CUFF CUWD	WGO1	0 ⟶ CSA	Continue Write: Delay ⟶ CS1
			1 ⟶ CECF	Arm Character Count for CS1
	$\overline{W9}$ CUFF CURD	WGO1	1 ⟶ CSB	Continue Read/Scan: Delay ⟶ CS7
	$\overline{W9}$ C12M SPGD	WGO1	1 ⟶ CSB	Continue Scan Reverse: Delay ⟶ CS7
	$\overline{CUFF}$ SPGD	WGO1	1 ⟶ CECF	Arm Clearing of Harvey Register in CS6
CS6: CSA CSB $\overline{CSC}$	CECF	FC	0 ⟶ (HR)	Clear Harvey Register
		WCP1	0 ⟶ CECF	Reset HR Clear Terminal
	$\overline{CECF}$	WGO1	(HR) + 1	Harvey Register Counts
			MTG = 1	Gap Signal to Buffer
	$\overline{HR05}$		STOP = 1	Stop Signal to Transport
	SPTD	WGO1	1 ⟶ CSRF	Set Buffer Halt Terminal
	CSRF		WHS = 1	Halt Signal to Buffer
	$\overline{W11}$		0 ⟶ CSA	Buffer Deselect: ⟶ CS0
			0 ⟶ CSB	
			0 ⟶ CECF	Idle-Ready
CS7: CSA CSB CSC	CUFF		1 ⟶ CERF	Enable Read
			1 ⟶ CFMF	Arm File Mark Detector
		WCP1	0 ⟶ CUFF	Reset Continue Flip-Flop
		RC	RF ⟶ (HR)	Read Signal into Harvey Register
	$\overline{C12M}$	RC	(HR) ⟶ Forward	Shift Harvey Register Forward
	C12M	RC	(HR) ⟶ Reverse	Shift Harvey Register Reverse
	RCP	FC	1 ⟶ CECF	Set Buffer Clock on Character
	$\overline{W5}$ $\overline{CSRF}$ CECF		ECM = 1	External Clock to Buffer
			(HR) ⟶ (R)	Transfer Character to Buffer
	W6	FC	0 ⟶ CECF	Reset Buffer Clock
	$\overline{SELS}$		WHS = 1	Tape Deselect (BOT): Halt Buffer
	$\overline{C12}$ $\overline{C13}$ $\overline{C14}$ C15 C16 $\overline{C17}$ C20	IOC	1 ⟶ CSRF	Set Skip-Remainder Flip-Flop
	W5 W6 $\overline{FMCD}$		0 ⟶ CFMF	Reset File Mark Flip-Flop
	$\overline{CUFF}$ (RSD + RSF) RG		0 ⟶ CERF	Detect Gap: ⟶ Disable Read
	$\overline{C12M}$ $\overline{CERF}$	WGO1	0 ⟶ CSB	Read/Scan Forward: ⟶ CS5
	C12M $\overline{CERF}$	WGO1	0 ⟶ CSB	Scan Reverse: ⟶ CS4
			0 ⟶ CSC	
	$\overline{CERF}$	WGO1	1 ⟶ CECF	Arm Clearing of Harvey Register in CS4 or CS5

Table 3-5. Tape Transport Unit Logic Equations

Function		Equation
$\overline{AANS}$	=	$\overline{LTD1} + \overline{LTN1} + \overline{LTD2} + \overline{LTN2}$
AUT	=	K2D AUTO Switch
$\overline{BOTS}$	=	BOT1 + BOT2
BRK1	=	$\overline{FWD1}\ \overline{REV1}\ \overline{REW1}$
BRK2	=	$\overline{FWD2}\ \overline{REV2}\ \overline{REW2}$
BTL	=	BOT
sCHSB	=	$(\overline{LTN1} + \overline{LTN2})$ (S12T + T12S)
rCHSB	=	$(\overline{LTD1} + \overline{LTD2})$ (S12T + T12S)
DATA	=	SEL1 + SEL2
$\overline{EOTS}$	=	EOT1 + EOT2
sEOT1	=	SBOT1 ETT1 $\overline{TSB1}$
rEOT1	=	TSB1 ETT1 + STOP Button + $\overline{K2D}$
sEOT2	=	SBOT2 ETT2 $\overline{TSB2}$
rEOT2	=	TSB2 ETT2 + STOP Button + $\overline{K2D}$
ETL1	=	$\overline{EOT1}$
ETL2	=	$\overline{EOT2}$
FWD1	=	TSA1 $\overline{TSB1}$
FWD2	=	TSA2 $\overline{TSB2}$
sK1	=	REW
rK1	=	$\overline{REW}$
sK2	=	$\overline{BOT}\ \overline{EOR}$ RESET Button
rK2	=	BOT + EOR
LWD1	=	SEL1 $\overline{CHSB}$ WRTS WED1
LWN1	=	SEL1 CHSB WRTS WEN1
LWD2	=	SEL2 $\overline{CHSB}$ WRTS WED2
LWN2	=	SEL2 CHSB WRTS WEN2
RDA1	=	TSB1 AUT1 RDY1
RDA2	=	TSB2 AUT2 RDY2

Table 3-5. Tape Transport Unit Logic Equations (Cont.)

Function		Equation
RDAS	=	DATA (LRD1 + LRN1 + LRD2 + LRN2)
RDD1	=	SEL1 $\overline{CHSB}$ AUT1
RDD2	=	SEL2 $\overline{CHSB}$ AUT2
RDN1	=	SEL1 CHSB
RDN2	=	SEL2 CHSB
$\overline{RDYS}$	=	$\overline{TSA1}$ RDA1 + $\overline{TSA2}$ RDA2
RDY1	=	AUT1 $(\overline{LTN1} + \overline{LTD1})$ $(\overline{BTS1} + \overline{BOT1})$
RDY2	=	AUT2 $(\overline{LTN2} + \overline{LTD2})$ $(\overline{BTS2} + \overline{BOT2})$
REV1	=	$\overline{TSA1}$ TSB1
REV2	=	$\overline{TSA2}$ TSB2
REW1	=	TSA1 TSB1
REW2	=	TSA2 TSB2
$\overline{SELS}$	=	SEL1 + SEL2
SEL1	=	AUT1 ($\overline{TSA1}$ TSB1 + TSA1 $\overline{TSB1}$ + SEL1 STOP)
SEL2	=	AUT2 ($\overline{TSA2}$ TSB2 + TSA2 $\overline{TSB2}$ + SEL2 STOP)
$\overline{TFPS}$	=	($\overline{LTN1}$ FPD1 + $\overline{LTD1}$ FPN1 + $\overline{LTN2}$ FPD2 + $\overline{LTD2}$ FPN2) K2C
sTSA1	=	RDY1 ($\overline{BOT1}$ REWM + T12S) + MAN1 K2D (FWD1 $\overline{EOT1}$ + REW1)
rTSA1	=	$\overline{TSB1}$ SEL1 STOP + MAN1 ($\overline{TSB1}$ EOT1 + REV1) + STOP Button + $\overline{K2D}$ + BOT1 $\overline{BOT1}$
sTSA2	=	RDY2 ($\overline{BOT2}$ REWM + T12S) + MAN2 K2D (FWD2 $\overline{EOT2}$ + REW2)
rTSA2	=	$\overline{TSB2}$ SEL2 STOP + MAN2 ($\overline{TSB2}$ EOT2 + REV2) + STOP Button + $\overline{K2D}$ + BOT2 $\overline{BOT2}$
sTSB1	=	RDY1 $\overline{BOT1}$ (REWM + S12T) + K2D MAN1 (REV1 + REW1)
rTSB1	=	$\overline{TSA1}$ SEL1 STOP + MAN1 FWD1 + $\overline{K2D}$ + STOP Button + BOT1 $\overline{BOT1}$
sTSB2	=	RDY2 $\overline{BOT2}$ (REWM + S12T) + K2D MAN2 (REV2 + REW2)
rTSB2	=	$\overline{TSA2}$ SEL2 STOP + MAN2 FWD2 + $\overline{K2D}$ + STOP Button + BOT1 $\overline{BOT1}$

This prevents any selection and starting of tapes on the 9248 when the 9448 is commanded. Further lockups in the 9248 occur when the 9448 is selected because the W11 line is held down:

$$W119 = W11\ \overline{CUG}$$

3-293 Thus, the 9248 can operate unmodified over the same channel with the 9448. A special test command, SKS1021n, permits the program to determine if a particular tape unit is a MAGPAK so that rewinds may be executed when switching tracks. The address acknowledge signal from the tape electronics unit is gated into the test reply line:

$$\overline{Sio} = \overline{C12}\ \overline{C13}\ \overline{C14}\ \overline{C15}\ C16\ AANS + - - -$$

Similarly, the 200-character/inch test is provided via AANS:

$$\overline{Sio} = C12\ C13\ \overline{C14}\ \overline{C15}\ C16\ AANS + - - -$$

3-294 GLOSSARY OF LOGIC TERMS

3-295 The mnemonics used in the 9446 Tape Transport Unit are basically three-letter mnemonics. (See table 3-6.) The fourth letter or digit indicates the use of the mnemonic. T Those ending with a 1 or 2 refer to tape station No. 1 or tape station No. 2. Most of the mnemonics ending in "S" refer to the common bus interrogation lines to the tape control unit. Those referring to the odd and even tape channels contain a "D" or "N" as the third letter. For example, the file protect line for the even channel of tape station No. 1 has the mnemonic FPN1.

3-296 Contained in tables 3-7 and 3-8 are logic equations and definitions for the 9448 Tape Control Unit.

Table 3-6. Definition of Logic Terms, Tape Transport Unit

Mnemonic	Definition
$\overline{AANS}$	Address acknowledge signal; pulled low when any tape station acknowledges the address
AUT1, AUT2	Tape station AUTO-MANUAL switch is in AUTO position; fault relay K2 is energized
BOR	Beginning-of-reel limit switch is closed; physical beginning-of-tape (right reel empty)
$\overline{BOTS}$	Beginning-of-tape status signal to tape control unit
BOT1, BOT2	Beginning-of-tape (beginning of portion of tape usable for data recording); photosense amplifier outputs
BRK1, BRK2	A line that goes low in order to activate the reel motor brakes. The brakes are on when motion is to cease; they remain on until motion is again impending. This line is released whenever a fault condition occurs
BTA1, BTA2	Beginning-of-tape photosensor anode
BRK1, BRK2	Beginning-of-tape photosensor cathode
BTL1, BRL2	Drive lines for the beginning-of-tape light (LOAD POINT indicator)
CHSB	Channel select flip-flop. It is set by either a forward or reverse command and an even channel addressed; it is reset by either a forward or reverse command and an odd channel addressed
DATA	Data select signal used to enable the read amplifier
EOR	End-of-reel limit switch closed; physical end of tape (left reel empty)
$\overline{EOTS}$	Signal to tape control unit indicating the end-of-tape flip-flop is set
EOT1, EOT2	End-of-tape flip-flops which are set when the end-of-tape marker is sensed and the unit is moving forward; they are reset by the end-of-tape marker being sensed while the unit is in reverse
ETA1, ETA2	End-of-tape photosenser anode

Table 3-6. Definition of Logic Terms, Tape Transport Unit (Cont.)

Mnemonic	Definition
ETK1, ETK2	End-of-tape photosensor cathode
ETL1, ETL2	Drive lines for END-OF-TAPE lights
ETT1, ETT2	End-of-tape photosense amplifier outputs used to set EOT1 or EOT2
FPD1, FPD2	File protect odd line from file protect switch
FPN1, FPN2	File protect even line from file protect switch
FWD1, FWD2	A line that is pulled low to energize the forward solenoid (which operates the forward pressure roller)
K1	Rewind relay (when energized, tape rewinds)
K2	Fault relay (when energized, no fault condition exists)
LLT0-LLT7	Unit select lines from the tape control unit
LRD1, LRD2	Logic read odd preamplifiers
LRN1, LRN2	Logic read even preamplifiers
$\overline{\text{LTD1}}$, $\overline{\text{LTD2}}$	Logic tape odd (ground for the active unit select lines)
$\overline{\text{LTN1}}$, $\overline{\text{LTN2}}$	Logic tape even (ground for the active unit select lines)
LWD1, LWD2	Logic write odd drivers
LWN1, LWN2	Logic write even drivers
MAN1, MAN2	Tape station is in manual mode of operation (AUTO-MANUAL switch is in MANUAL)
PLP1, PLP2	Photosense lamp supply lines
RDA1, RDA2	Read data signals
RDAS	Output of the read amplifier after shaping
RDD1, RDD2	Read data odd (gated with the lines from the read heads)
RDK	Read odd wire from the read head (black)
RDL1, RLD2	Drive lines for READY indicators
RDN1, RDN2	Read data even (gated with the lines from the read heads)
RDR	Read odd wire from the read head (red)
$\overline{\text{RDYS}}$	Select ready signal to the tape control unit which indicates there is no motion, the unit is in automatic, there is no stop delay, and the K2 relay is energized
RDY1, RDY2	Tape station ready signal indicating the unit will accept a command if addressed

Table 3-6. Definition of Logic Terms, Tape Transport Unit (Cont.)

Mnemonic	Definition
REV1, REV2	A line from a relay driver to the reverse solenoid which is pulled low to operate the reverse pressure roller
REW1, REW2	A line which is pulled low to energize the rewind relay, K1
REWM	Rewind command from the tape control unit; it goes to all tape stations on the line, but only the tape station that is addressed will interpret and operate on the command
RNG	Read even wire from the read head (gray)
RNU	Read even wire from the read head (blue)
$\overline{\text{RTRN}}$	Return line for the AUTO-MANUAL switch
SEL1, SEL2	Signal indicating that a tape station is in automatic, has been addressed, tape is in motion (but not rewinding), and data can be expected to be either read or written on that particular tape station
$\overline{\text{SELS}}$	Select signal to the tape control unit indicating that a tape station has been selected and is expected to transmit or receive data
STOP	Signal from the STOP switch which is used to reset the TSA and TSB flip-flops
S12T	Reverse start command signal to all tape stations; only the tape station addressed will respond
$\overline{\text{TFPS}}$	Tape file protect signal to the tape control unit which (when pulled down) indicates that a channel which has been selected is file protected
TSA1, TSA2	Tape station "A" flip-flop used to control tape motion; it is true for either forward or rewind operation
TSB1, TSB2	Tape station "B" flip-flop used to control tape motion; it is true for either rewind or reverse operation
T12S	Forward start command signal to all tape stations; only the tape station addressed will respond
WED1, WED2	Write enable odd signal derived from the file protect switch
WEN1, WEN2	Write enable even signal derived from the file protect switch
WDAS	Write data signal from the tape control unit
WDG1, WDG2	Write odd wire from the write head (green)
WDW1, WDW2	Write odd wire from the write head (white)
WNB1, WNB2	Write even wire from the write head (brown)
WNY1, WNY2	Write even wire from the write head (yellow)
WRTS	Write select control signal from the tape control unit

Table 3-7. Tape Control Unit Logic Equations

EQUATION	NOTES
Write Logic Section Equations	
Write Clock Generator	
jWCA = WCB WCD	
kWCA = WCB WCD	
jWCB = WCC WCD	
kWCB = WCD	
jWCC = $\overline{\text{WCB}}$ WCD	
kWCC = WCD	
jWCD = CSG	
kWCD = CSG	
cWCA = cWCB = cWCC = cWCD = $\underline{\text{FC}}$	
rWCA = rWCB = rWCC = rWCD = ($\overline{\text{W11}}$) dc	
Write Clock Outputs	
WCP0 = $\overline{\text{WCA}}$ WCB WCD CSG FC	
WCP1 = WCA WCB WCD CSG FC	
Write Synchronizer	
jWSA = WSB WSC CSG	
kWSA = WSB CSG	
jWSB = WSC CSG	
kWSB = (WSA + WSC) CSG	
jWSC = ($\overline{\text{WSA}}$ + $\overline{\text{WSB}}$) CSG	
kWSC = WSC CSG	
cWSA = cWSB = cWSC = $\underline{\text{WCP0}}$	
rWSA = rWSB = rWSC = ($\overline{\text{W11}}$) dc	
Write Character Gate	
WGO1 = WSA WSB WCP0	

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION	NOTES
Write Logic Section Equations (Cont.)	
Write Flip-Flop	
jWF = kWF = W9 CSG	
cWF = WCP1	Sync
+ CS1 $\overline{\text{CECF}}$ WSA WSB WCP0	Preamble
+ CS2 $\overline{\text{HR00}}$ WCP0	Write
+ CS3 CECF $\overline{\text{WSA}}$ $\overline{\text{WSB}}$ $\overline{\text{WSC}}$ WCP0	Postamble
rWF = $\overline{(\text{W11})}$ dc	
Read Logic Section Equations	
Read Signal Standardizer	
dRSF1 = RDAS $\overline{\text{TEST}}$	Normal
+ WDAS TEST	Back-to-Back Test
dRSF2 = RSF1	
cRSF1 = cRSF2 = FC	Reference Clock
rRSF1 = rRSF2 = STRT	Initialize
gRSF1 = gRSF2 = CERF	Enable
Standardized Read Pulses	
RSF3 = $\overline{\text{RSF1}}$ RSF2 + RSF1 $\overline{\text{RSF2}}$	
Read Flip-Flop	
jRF = RDA RSF3	Arm
kRF = $\overline{\text{RDA}}$ RSF3	Reset for Zero
cRF = FC	
Read Clock	
RC = RSF3 RDA FC	
Read Gap	
RG = $\overline{\text{RSF3}}$ RDA RDB RDC RDD	Late Transition
+ RSF3 $\overline{\text{RDA}}$ $\overline{\text{RDB}}$ ($\overline{\text{RDC}}$ + $\overline{\text{RDD}}$)	Early Transition

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION	NOTES
Read Logic Section Equations (Cont.)	
Read Decoder	
jRDA = RDB RDC RDD	
kRDA = RSF3	
jRDB = $(\overline{RSF3} + \overline{RDA})$ RDC RDD	
kRDB = RSF3 RDA + $\overline{RDA}$ RDC RDD	
jRDC = $(\overline{RSF3} + \overline{RDA})$ RDD	
kRDC = RSF3 RDA + $(\overline{RDA} + \overline{RDB})$ RDD	
jRDD = $\overline{RSF3} + \overline{RDA}$	
kRDD = RSF3 + $\overline{RDA}$ + $\overline{RDB}$ + $\overline{RDC}$	
cRDA = cRDB = cRDC = cRDD = $\underline{FC}$	
Read Synchronizer (Counter)	
jRSA = RSB RSC (RSD + RSF + RF) $\overline{RG}$	
kRSA = RSB RSD + $\overline{RF}$ RSB $\overline{RSF}$ + RG	
jRSB = RSC (RSD + RSF + RF) $\overline{RG}$	
kRSB = RSC (RSD + RSF + RF) $\overline{RG}$ + RSA RSD + $\overline{RF}$ RSA $\overline{RSF}$ + RG	
jRSC = $(\overline{RSA} + \overline{RSB})$ $\overline{RG}$	
kRSC = RSC (RSD + RSF + RF) + RG	
cRSA = cRSB = cRSC = $\underline{RC}$ + RG $\underline{FC}$	
rRSA = rRSB = rRSC = (CS0) dc	
Preamble Detector	
jRSD = $\overline{RF}$ RSA RSB $\overline{RSF}$ $\overline{RG}$	
kRSD = RF RSA RSB RSF + RG	
cRSD = $\underline{RC}$ + RG $\underline{FC}$	
rRSD = (CS0 + $\overline{CERF}$ FC) dc	

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION	NOTES
Read Logic Section Equations (Cont.)	
Parity Error Detector	
jRSE = RSD $\overline{RF}$ $\overline{RG}$	
kRSE = CERF $\overline{RF}$ RSD	
cRSE = RC + RG FC	
rRSE = (STRT + $\overline{CERF}$ FC) dc	
gRSE = CERF	
Postamble Detector	
jRSF = $\overline{RF}$ RSA $\overline{RSB}$ $\overline{RSC}$ RSD $\overline{RG}$	
kRSF = $\overline{RF}$ RSD CERF	
cRSF = RC + RG FC	
rRSF = (STRT + $\overline{CERF}$ FC) dc	
gRSF = CERF	
Read Character Pulse	
RCP = RSA RSB RSD ($\overline{RSF}$ + $\overline{RF}$) RC	
Read Error Signal	
RES = RG RSD FC	Gap in Data (01-32-31)
+ RSE $\overline{RSA}$ $\overline{RSB}$ $\overline{RSC}$ $\overline{RSF}$	Parity Error (01-32-22)
+ RSA RSB $\overline{RSD}$ RSF	Premature Postamble (01-32-18)
Harvey Register Section Equations	
Harvey Register Control	
Shift Forward Gate	
SFG = CS27 $\overline{C12M}$ $\overline{CECF}$	CS2 + CS7
Shift Reverse Gate	
SRG = CS27 C12M $\overline{CECF}$	CS2 + CS7
Shift Parallel Gate	
SPG = CS2 CECF	CS2

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION	NOTES
Harvey Register Section Equations (Cont.)	
Harvey Register Control (Cont.)	
Count Binary Gate	
CBG = CS0	CS0
+ (CS4 + CS56) $\overline{\text{CECF}}$	CS4, 5, 6
Serial Shift Pulse	
SSP = CS2 WCP0	Write
+ CS7 RC	Read
Shift Parallel Pulse	
SPP = $\overline{\text{CS0}}$ $\overline{\text{CS7}}$ CECF FC	Output from Buffer and HR Clearing
Harvey Register Gate	
HRG = $\overline{\text{SFG}}$ $\overline{\text{SRG}}$ $\overline{\text{SPG}}$ $\overline{\text{CBG}}$	Inverter Control
Harvey Register Inputs	
dHR00 = SFG HR01 + SRG RF + SPG RP + CBG $\overline{\text{HR00}}$	
dHR01 = SFG HR02 + SRG HR00 + SPG R1 + CBG $\overline{\text{HR01}}$	
dHR02 = SFG HR03 + SRG HR01 + SPG R2 + CBG $\overline{\text{HR02}}$	
dHR03 = SFG HR04 + SRG HR02 + SPG R3 + CBG $\overline{\text{HR03}}$	
dHR04 = SFG HR05 + SRG HR03 + SPG R4 + CBG $\overline{\text{HR04}}$	
dHR05 = SFG HR06 + SRG HR04 + SPG R5 + CBG $\overline{\text{HR05}}$	
dHR06 = SFG HRIN + SRG HR05 + SPG R6 + CBG $\overline{\text{HR06}}$	
HRIN = $\overline{\text{W9}}$ RF + W9 HR00	Recirculate for file mark
Harvey Register Clocks	
cHR00 = SSP + SPP + CBG WG01	
cHR01 = SSP + SPP + CBG HR00	
cHR02 = SSP + SPP + CBG HR01	
cHR03 = SSP + SPP + CBG HR02	
cHR04 = SSP + SPP + CBG HR03	

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION	NOTES
Harvey Register Section Equations (Cont.)	
Harvey Register Clocks (Cont.)	
cHR05 = SSP + SPP + CBG HR04	
cHR06 = SSP + SPP + CBG HR05	
rHR00 = rHR01 = - - - = rHR06 = ($\overline{W11}$) dc	
Harvey Register Outputs	
Delay Definitions	
STGD = HR05 HR04 HR02 HR00 WGO1	START GAP DELAY — 36 milliseconds
WTRD = HR05 HR04 HR01 HR00 WGO1	WRITE TO READ DELAY - 34.7 ms OR 37.4 OR 4 CR 4.
SPGD = HR05 HR02 HR01 WGO1	STOP GAP DELAY - 26 milliseconds
SPTD = HR05 HR03 HR02 HR00 WGO1	STOP TAPE DELAY - 30.7 milliseconds
CUWD = HR06 HR04 HR03 HR01 WGO1	CONTINUE WRITE DELAY - 60.7 milliseconds
IHGD = HR06 HR03 HR01 HR00 WGO1	INTER HEAD GUARD DELAY - 30.7 milliseconds
CURD = HR06 HR05 HR04 HR03 WGO1	CONTINUE READ DELAY 75.5 ms
File Mark Detect	
FMCD = HR00 $\overline{HR01}$ $\overline{HR02}$ HR03 HR04 HR05 HR06	IT'S # PARITY
Control Logic Section Equations	
Control State Counter	
jCSA = CS0 IHGD	Read/Scan Forward: CS0 → CS7
+ CS0 $\overline{W9}$ C12M	Scan Reverse: CS0 → CS7
+ CS3 $\overline{CECF}$	Write/Erase: CS3 → CS4, 5
kCSA = CS5 W9 CUFF CUWD	Write Continue: CS5 → CS1
jCSB = CS0 IHGD	Read/Scan Forward: CS0 → CS7
+ CS0 $\overline{W9}$ C12M	Scan Reverse: CS0 → CS7
+ CS1 $\overline{CECF}$	Write/Erase: CS1 → CS2
+ CS4 W10 IHGD	Erase Reverse: CS4 → CS6
+ CS5 SPGD $\overline{CUFF}$	Non Continue: CS5 → CS6
+ CS5 $\overline{W9}$ C12M SPGD	Scan Reverse: CS5 → CS7
+ CS5 CUFF CURD	Read Continue: CS5 → CS7

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION	NOTES
Control Logic Section Equations (Cont.)	
Control State Counter (Cont.)	
kCSB = CS3 $\overline{\text{CECF}}$	Write/Erase: CS3 → CS4, 5
+ CS7 $\overline{\text{CERF}}$	Read/Scan: CS7 → CS4, 5
jCSC = CS0 W9 STGD	Write/Erase: CS0 → CS1
+ CS0 $\overline{\text{W9}}$ C12M	Scan Reverse: CS0 → CS7
+ CS0 IHGD	Read/Scan Forward: CS0 → CS7
+ CS2 W5 CUFF	Write/Erase: CS2 → CS3
+ CS2 W5 CFMF	Write File Mark: CS2 → CS3
+ CS4 W9 $\overline{\text{W10}}$ $\overline{\text{CERF}}$ WTRD	Write: CS4 → CS5
+ CS4 $\overline{\text{W9}}$ WTRD	Scan Reverse: CS4 → CS5
+ CS4 $\overline{\text{W10}}$ IHGD	Write: CS4 → CS5
kCSC = CS1 $\overline{\text{CECF}}$	Write/Erase: CS1 → CS2
+ CS3 $\overline{\text{W10}}$ $\overline{\text{CECF}}$	Write: CS3 → CS4
+ CS3 C12M $\overline{\text{CECF}}$	Erase Reverse: CS3 → CS4
+ CS5 SPGD $\overline{\text{CUFF}}$	Non Continue: CS5 → CS6
+ CS7 C12M $\overline{\text{CERF}}$	Scan Reverse: CS7 → CS4
rCSA = rCSB = rCSC = ($\overline{\text{W11}}$ $\overline{\text{STRT}}$) dc	Any State CS0
cCSA = cCSB = cCSC = $\underline{\text{WGO1}}$	Character-Time Clock
Control State Definitions	
CS0 = $\overline{\text{CSA}}$ $\overline{\text{CSB}}$ $\overline{\text{CSC}}$	Start
CS1 = $\overline{\text{CSA}}$ $\overline{\text{CSB}}$ CSC	Preamble
CS2 = $\overline{\text{CSA}}$ CSB $\overline{\text{CSC}}$	Write
CS3 = $\overline{\text{CSA}}$ CSB CSC	Postamble
CS4 = CSA $\overline{\text{CSB}}$ $\overline{\text{CSC}}$	Interhead
CS5 = CSA $\overline{\text{CSB}}$ CSC	Gap
CS6 = CSA CSB $\overline{\text{CSC}}$	Stop
CS7 = CSA CSB CSC	Read

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION			NOTES
Control Logic Section Equations (Cont.)			
Control State Definitions (Cont.)			
CS13	=	$\overline{CSA}$ CSC	Preamble/Postamble (CS1 + CS3)
CS27	=	CS2 + CS7	Write/Read
CS56	=	CS5 + CS6	Gap/Stop
Control Select Gate			
CSG	=	CSA + CSB + CSC + CECF	Out of Idle-Ready
External Clock Flip-Flop			
iCECF	=	CS0 $\overline{STRT}$ SELS	Depart Idle-Ready
		+ CS13 WGO1	Preamble/Postamble Character Count
		+ CS2 (CUFF + CFMF) WGO1	Write/Erase: Clock to Buffer
		+ CS4 $\overline{CERF}$ WTRD $\overline{W9\ W10\ C12M\ SELS}$	Arm HR Clearing in CS5, 6
		+ CS4 IHGD	
		+ CS5 $\overline{CUFF}$ SPGD	Arm HR Clearing in CS6
		+ CS5 W9 CUFF CUWD	Arm HR Clearing in CS1
		+ CS7 RCP	Read/Scan: Clock to Buffer
		+ CS7 $\overline{CERF}$ WGO1	Arm HR Clearing in CS4, 5
kCECF	=	CS0 $\overline{W9}$ C12M WGO1	Scan Reverse: Reset Clock
		+ CS0 IHGD	Read/Scan Forward: Reset Clock
		+ CS13 WGO1	Preamble/Postamble Character Count
		+ (CS4 + CS5 + CS6) WCP1	HR Clearing Complete
		+ CS27 W6	Reset Clock to Buffer
sCECF	=	(CS1 W10 C12M RG + FC CS4 RSA RSB C12M) dc	Scan/Erase over Gap
rCECF	=	($\overline{W11}$ $\overline{STRT}$) dc	Hold in Idle-Ready
cCECF	=	FC	Reference Clock
Control Logic DC Flip-Flops			
Tape Reverse Monitor FF			
sC12M	=	STRT C12	Set for Reverse
rC12M	=	$\overline{W11}$	Clear Reverse

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION			NOTES
Control Logic Section Equations (Cont.)			
Control Logic DC Flip-Flops (Cont.)			
Erase Tape FF			
sCETF	=	CS0 W9 W11 WCP1	Write/Erase: Begin Erase
		+ CS3 $\overline{\text{CECF}}$ WSB WCP1	Terminate Postamble
rCETF	=	CS1 $\overline{\text{W10}}$ WSA WSC WCP1	Commence Preamble
Enable Read FF			
sCERF	=	CS13	Write/Erase: Enable Read
		+ CS7 CUFF	Read: Enable Read
rCERF	=	CSA $\overline{\text{CUFF}}$ (RSD + RSF) RG FC	CS4, 5, 6, 7: Disable on Gap
		+ $\overline{\text{W11}}$	Disable Read
sCUFF	=	CS2 $\overline{\text{W5}}$ WSB WCP1	Normal Write Detect
		+ CS5 STRT	Remember Continue Command
		+ $\overline{\text{W11}}$	Arm for CERF, CFMF in CS7
rCUFF	=	CS13	Write: Reset for CS2, CS5
		+ CS7 WCP1	Complete Setting of CERF, CFMF
Skip Remainder FF			
sCSRF	=	CS2 $\overline{\text{CUFF}}$ WGO1	Write: Count First Character
		+ CS6 SPTD	Remember Buffer Halt in CS0
		+ CS7 CNTL ($\overline{\text{C12}}$ C13 C14 C15 C16)	Disable Clocks to Buffer
rCSRF	=	$\overline{\text{CSB}}$ WCP1	CS0, 1, 4, 5: Reset for CS2, 6, 7
		+ STRT $\overline{\text{Q2}}$ $\overline{\text{SELS}}$	Detect 9248 Selection
File Mark FF			
sCFMF	=	CS2 W5 CSRF WSA WCP1	Write File Mark: Second Character
		+ CS7 CUFF	Read File Mark: Arm
rCFMF	=	CS13	Write: Reset for CS2
		+ CS7 W5 W6 $\overline{\text{FMCD}}$	Read File Mark: Detect
		+ RSD RG FC	Defeat File Mark if Gap in Record
		+ STRT	Reset if 9248 Selected

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION	NOTES
Control Tape Logic Equations	
Logical Tape Transport Address	
LLT0 = $\overline{C21}\ \overline{C22}\ \overline{C23}$	
LLT1 = $\overline{C21}\ \overline{C22}\ C23$	
LLT2 = $\overline{C21}\ C22\ \overline{C23}$	
LLT3 = $\overline{C21}\ C22\ C23$	
LLT4 = $C21\ \overline{C22}\ \overline{C23}$	
LLT5 = $C21\ \overline{C22}\ C23$	
LLT6 = $C21\ C22\ \overline{C23}$	
LLT7 = $C21\ C22\ C23$	
Start/Control Signals	
STRT = Buc $\overline{C17}$ C20	Buffer Unit EOM
CNTL = Ioc $\overline{C17}$ C20	I/O Control EOM
Tape Motion Control Signals	
T12S = STRT $\overline{C12}$ Q2	Start Forward
S12T = STRT C12 Q2	Start Reverse
REWM = CNTL C12 $\overline{C16}$ $\overline{TEST}$	Start Rewind
STOP = $\overline{HR05}$ CS6 + $\overline{W11}$ $\overline{STRT}$	Stop Forward/Reverse
Write Data/Control	
WRTS = W9 SELS	Write Control
WDAS = $\overline{CETF}$ WF	Write Data
Control-Computer Logic Equations	
Character Transfer to Buffer	
$\overline{ZW1}$ = $\overline{CS7\ HR01}$	
$\overline{ZW2}$ = $\overline{CS7\ HR02}$	
$\overline{ZW3}$ = $\overline{CS7\ HR03}$	
$\overline{ZW4}$ = $\overline{CS7\ HR04}$	
$\overline{ZW5}$ = $\overline{CS7\ HR05}$	
$\overline{ZW6}$ = $\overline{CS7\ HR06}$	
$\overline{ZWP}$ = $\overline{CS7\ HR00}$	

Table 3-7. Tape Control Unit Logic Equations (Cont.)

EQUATION	NOTES
Control-Computer Logic Equations (Cont.)	
Clock To Buffer	
(Ecw) = $\overline{CS27\ CERF\ \overline{CSRF}\ CECF + ECM9}$	
Halt to Buffer	
Whs = $\overline{CS6\ CSRF + \overline{CS0}\ \overline{CS56}\ \overline{SELS}\ \overline{TEST}}$	
$+ \overline{\overline{SELS}\ AANS\ \overline{Q2}\ STRT + WHS9}$	
Magnetic Tape Gap to Buffer	
(Mtg) = $CS56\ \overline{CUFF} + MTG9$	
Error Signal to Buffer	
(Wes) = $\overline{RES + \overline{SELS}\ WES9}$	
Skip Logic	
(Sio) = $C17 + \overline{C20}$	Magnetic Tape Inquiry
$+ C15\ \overline{C16}\ CS0\ RDYS$	Control/Tape Ready
$+ C12\ \overline{C16}\ TFPS$	Tape File Protect
$+ C13\ \overline{C16}\ BOTS$	Beginning of Tape
$+ C14\ \overline{C16}\ EOTS$	End of Tape
$+ C12\ C13\ \overline{C14}\ \overline{C15}\ C16\ AANS$	Tape Density 200 BPI
$+ \overline{C12}\ C13\ \overline{C14}\ C15\ CS5\ \overline{CUFF}\ \overline{CFMF}$	Control Gap
$+ \overline{C12}\ C13\ C14\ C15\ C16\ CUG\ CFMF$	9448 File Mark
$+ \overline{\overline{C12}\ C13\ C14\ C15\ C16\ CUG\ \overline{SIO9}}$	9248 Responses
$+ \overline{C12}\ \overline{C13}\ \overline{C14}\ \overline{C15}\ C16\ AANS$	MAGPAK
Auxiliary-Control Logic Equations for 9248	
Control Gate	
CUG = $CSA + CSB + CSC + CECF + CSRF$	Indicate 9448 selected or was last selected
Interposed Terms	
$\overline{C179}$ = 1	Forces 9248 M start true when 9448 selected and reading
C209 = 1	
BUC9 = STRT + CS7	
IOC9 = CNTL	Permit Rewind through 9248
Q29 = $\overline{Q2}\ \overline{CUG}$	Block Q2 to 9248
W119 = $W11\ \overline{CUG}$	Block 9248 Selection

Table 3-8. Definition of Logic Terms, Tape Control Unit

Mnemonic	Definition
AANS	Address acknowledge signal from 9446 tape unit used to respond to tape density tests
BOTS	Beginning of tape signal from addressed unit
BUC	Buffer unit control signal (Buc) used to strobe EOM commands
BUC9	Auxiliary BUC to 9248 connector
CBG	Count binary gate. Conditions the Harvey register to provide time delays by counting WGO1 pulses
CECF	External clock flip-flop. Provides Ecw signal to buffer and is time-shared to perform other control functions
CERF	Enable read flip-flop; also used in gap detector
CETF	Erase tape flip-flop
CFMF	File mark flip-flop
CNTL	Control signal for magnetic tape decoded from computer IOC command
CSA-CSC	Control state counter
CSG	Control selected gate indicating that 9448 has been taken out of idle-ready by an STRT from the computer buffer
CSRF	Skip remainder flip-flop; time-shared for remembering that the last command given was to a MAGPAK
CS0-CS7	Control States:
CS0	IDLE-START
CS1	PREAMBLE
CS2	WRITE
CS3	POSTAMBLE
CS4	INTERHEAD
CS5	GAP
CS6	STOP-HALT
CS7	READ
CS13	Control States CS1 or CS3. Indicates that preamble or postamble is being written
CS27	Control States CS2 or CS7. Indicates that writing or reading of characters is taking place
CS56	Control States CS5 or CS6. Indicates that a shutdown sequence is in progress
CUFF	Continue Flip-Flop

Table 3-8. Definition of Logic Terms, Tape Control Unit (Cont.)

Mnemonic	Definition
CUG	Control Unit Gate. Indicates that 9448 is selected or that the 9248 is not selected
CURD	Continue Read Delay (75.5 ms)
CUWD	Continue Write Delay (60.7 ms)
C12-C23	Computer C Register signals used to control 9448
C12M	Reverse Monitor Flip-Flop. Stores C12 throughout tape operation
ECM	Clock to Computer Buffer (Ecm). For W-Buffer, this term is represented as ECW.
ECW	See ECM
EOTS	End-of-Tape signal from addressed tape unit
FC	Reference Clock. Crystal-controlled oscillator, operating at 126 Kc (12 times the MAGPAK bit-rate)
FMDG	File Mark Detect Gate
HRG	Harvey Register Gate used to qualify inverter logic
HR00-HR06	Seven-Stage Harvey Register. Converts serial/parallel and parallel/serial, and provides all MAGPAK timing terms by acting as a binary computer
IHGD	Interhead Guard Delay (50.7 ms)
IOC	Input/Output Control signal (Ioc). Used to strobe EOM commands
IOC9	Auxiliary IOC to 9248 connector
LLT0-LLT7	Logical Tape Unit addresses decoded from C21-C23
MTG	Magnetic Tape Gap signal (Mtg) to Computer Buffer
MTG9	Auxiliary MTG signal from 9248 connector
Q2	Computer pulse counter signal
Q29	Auxiliary Q2 to 9248 connector
RC	Read Clock derived in RDA-RDD, used to strobe RF
RCP	Read Character Pulse, derived in RSA-RDS, coincident with every 7th RC signal after character sync is established
RDA-RDD	Read Decoder Flip-Flops. Act as variable period binary counter clocked by FC
RDAS	Read Data Signal from 9246 electronic unit
RDYS	Ready Signal from addressed transport
RES	Read Error Signal
REWM	Rewind Control signal to addressed transport
RF	Read Flip-Flop. Converts FM signal from tape to serial binary
RG	Read Gap. Indicates gap condition detected by RDA-RDD
R1-R6, RP	Computer Buffer parallel output signals
RSA-RSC	Read Synchronizer Flip-Flop, used as seven-state binary bit-time counter clocked by RC

Table 3-8. Definition of Logic Terms, Tape Control Unit (Cont.)

Mnemonic	Definition
RSD	Read Synchronizer Flip-Flop, used to detect preamble and control/character reading
RSE	Read Synchronizer Flip-Flop, used to detect serial odd parity errors
RSF	Read Synchronizer Flip-Flop, used to detect and confirm the postamble
RSF1-RSF2	Read Standardizer Flip-Flops. Act as shift register for RDAS signal clocked by FC
RSF3	Standardized Read signal transitions formed by gating between RSF1 and RSF2
SELS	Select Signal from 9446, indicating that addressed transport is selected
SFG	Shift Forward Gate to Harvey Register
SIO	Response from I/O device (Sio) to SKS instructions
SIO9	Auxiliary SIO signal from 9248 connector
SPG	Shift Parallel Gate to Harvey Register
SPGD	Stop Gap Delay (26.0 ms); allows time for Continue Flip-Flop, CUFF, to set if continue option is desired
SPTD	Stop Tape Delay (30.7 ms); maintains current in write heads until tape stops
SRG	Shift Reverse Gate to Harvey Register
STGD	Start Gap Delay (36.0 ms); allows time for tape to start and travel 0.225 inch
STOP	Stop signal to 9446 to halt tape motion
STRT	Magnetic Tape Start signal decoded from Computer BUC command
S12T	Start Tape Motion in Reverse command to addressed transport
TEST	Control signal which, when grounded, causes data to be coupled back-to-back, write to read, and prevents tape motion commands
TFPS	File Protect signal from 9446 indicating switch position on addressed transport.
T12S	Start Tape Motion Forward command to addressed transport
WCA-WCD	Write Clock Generator Flip-Flops, operating as a twelve-state counter clocked by FC
WCP0	Write Clock Phase Zero, pulse derived in WCA-WCD. Indicates time to write zero transition
WCP1	Write Clock Phase One, pulse derived in WCA-WCD. Indicates time to write synchronizing transition
WDAS	Write Data Signal to selected transport
WES	Error Signal to Computer Buffer (Wes)
WF	Write Flip-Flop. Converts serial binary to FM recording format
WGO1	Write Character Pulse derived in WSA-WSC
WHS	Halt Signal to Computer Buffer (Whs)
WRTS	Write Control Signal to 9446
WSA-WSC	Write Synchronizer operating as a seven-state binary counter clocked by WCP0
WTRD	Write to Read Delay (34.7 ms)
W0	W-Buffer Flip-Flop signal in controlling termination of data transfer
W5	W-Buffer Precess Detector, participates in halt interlock
W6	W-Buffer Flip-Flop signal used to acknowledge Ecw

Table 3-8. Definition of Logic Terms, Tape Control Unit (Cont.)

Mnemonic	Definition
W9	W-Buffer Flip-Flop signal indicating an output operation
W10	W-Buffer Flip-Flop signal indicating erase or scan operations
W11	W-Buffer Flip-Flop designates magnetic tape operations
ZW1-Zw6, ZWP	Computer Buffer parallel input lines (Zw1-Zw6, Zwp)

SECTION IV
INSTALLATION AND MAINTENANCE

4-1 INSTALLATION

4-2 Basically, the Model 9446 Tape Transport Unit can either be installed in a standard 19-inch relay rack or mounted on a table (such as the SDS Model 92360 Table). The Model 9448 Tape Control Unit is always rack-mounted.

4-3 These units are shipped either mounted in cabinets or packed in individual, custom-built, packing boxes. In either case, both units can be stored, shipped, or handled in any orientation. Normal unpacking procedures for this type of equipment should be followed; packing cases should be opened carefully and their contents examined for damage incurred during shipment. If the units are to be moved or reshipped, packing similar to that in which the units were received will be adequate.

4-4 Tables 4-1 and 4-2 list the environmental specifications and power requirements applicable to installation of a MAGPAK tape system. Refer to section I of this manual for a complete list of MAGPAK specifications. Figures 4-1, 4-2, and 4-3 show the dimensions for the Model 9446 Tape Transport Unit, Model 9402 Dust Cover Housing, and Model 92360 Table, respectively. Refer also to the installation drawings included in section V of this manual.

Table 4-1. MAGPAK Environmental Specifications

Item	Specification
Operating Temperatures	10°C-40°C (50°F-104°F)
Operating Humidity	20% - 80% RH
Heat Dissipation	
9446	900 BTU per hour
9448	450 BTU per hour
Weight	
9446	75 lb (without dust cover)
9448	75 lb
9402 Dust Cover	25 lb
92360 Table	65 lb
Recommended Access Area	3 ft in front and rear of table or cabinet

Table 4-2. MAGPAK Power Requirements

Item	Specification	
	Model 9446	Model 9448
Power Requirements		
115 vac ±10%, 60 cps ±3 cps	2.0 amps	
+50 vdc	0.4 amp	
+25 vdc	1.0 amp	3.4 amps
+ 8 vdc	1.6 amps	1.6 amps
-25 vdc	0.2 amp	0.4 amp
Recommended AC Service	115 vac, 5 amps per Model 9446	
AC Service Receptacle	Hubbell type 5262 FE polarized, or equivalent	
Power Cable Lengths	AC: 8 ft	
	DC: 20 ft (std) 5 or 10 ft (optional)	DC: 5 ft

4-5 INSTALLATION PROCEDURE

4-6 Model 9446

4-7 Rack-Mounted. Mount the 9446 assembly in the 19-inch rack with the hardware provided. Adapters are available for 24-inch rack mounting. Cable lengths and interconnection requirements must be considered when determining the location of the 9446 assembly.

4-8 Table-Mounted. When the tape transport unit is mounted on a table top, the unit must be enclosed in a Model 9402 Dust Cover Housing. Since the dust cover contains a fan in the base for air circulation, the rubber feet on the base should not be removed. If they are, a hole must be cut in the table top to provide for air flow.

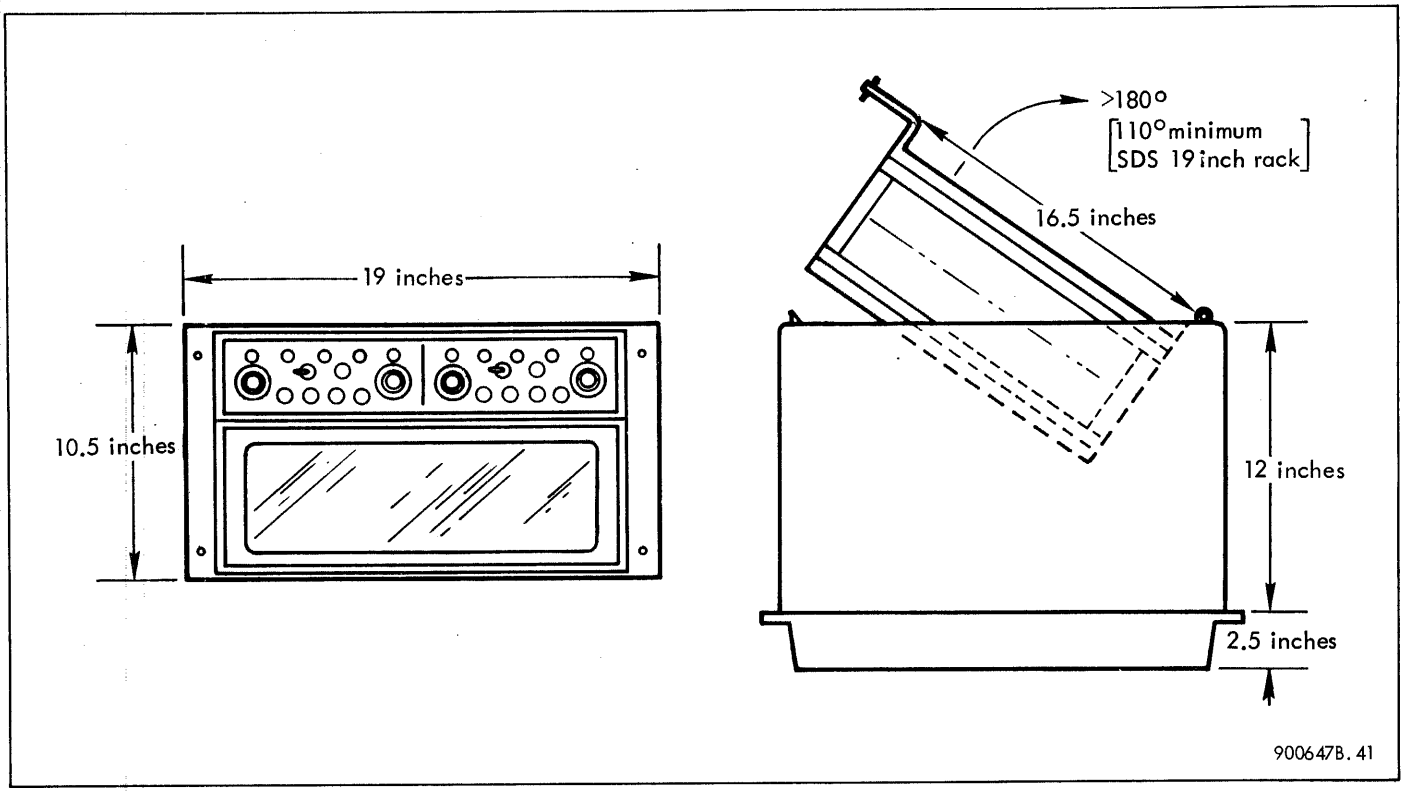


Figure 4-1. Model 9446 Tape Transport Unit Dimensions

4-9 Up to two tape transport units may be counted on each Model 92360 Table. The table has a vertical cable trough in the right-hand rear corner, as shown in figure 4-3. Receptacles beneath the table connect ac power to the tape transport units. Line power is connected to the receptacles by a 20-foot-long cable.

4-10 Model 9448

4-11 Mount the 9448 assembly in the 19-inch rack with the hardware provided. Adapters are available for 24-inch rack mounting. Cable lengths and interconnection requirements must be considered when determining the location of the 9448 assembly.

4-12 INTERCONNECTING CABLING

4-13 Interconnecting cabling for the MAGPAK Tape System is shown in figure 4-4. Refer to this figure and perform the following steps:

a. Install Cable Plug Module P82 from left tape station in location J41 of 9446 Tape Transport Unit electronics (designated chassis 00).

b. Install P82 from right tape station in J42-00. Both P82 cables are 3 feet long. (Note that P82 from either the left or right tape station can be plugged into either J41 or J42 of the 9446 electronics; the tape stations will perform exactly alike regardless of which position they are plugged in. Usually the tape station cable plug modules are connected as shown in figure 4-4.)

c. Install P84 in J26-00; install P83 in J42 of 9448 Tape Control Unit chassis 03.

d. Install P81 in J44-03; install P80 in magnetic tape control connector of computer I/O buffer. The P80-P81 cable is 5 feet long.

e. If additional 9446 Tape Transport Units are to be operated from the same 9448 Tape Control Unit, install P83 in location J27-00 of the preceding tape transport unit. The P83-P84 cable lengths and part numbers are shown in table 4-3. Any combination of cables may be used, but the total length of all P83-P84 cables must not exceed 47 feet for standard MAGPAK tape systems.

f. If the I/O buffer used has time-sharing capabilities, an SDS Model 9248 Magnetic Tape Control Unit (or equivalent) can be operated from the same buffer channel. For this arrangement, remove Termination Module ZX49 from 9448 Tape Control Unit chassis location J41-03, and install Cable Plug Module P40 from 9248 (or equivalent) unit.

g. Connect 9446 dc power cable wires to appropriate computer power buses as indicated in table 4-3. The wires

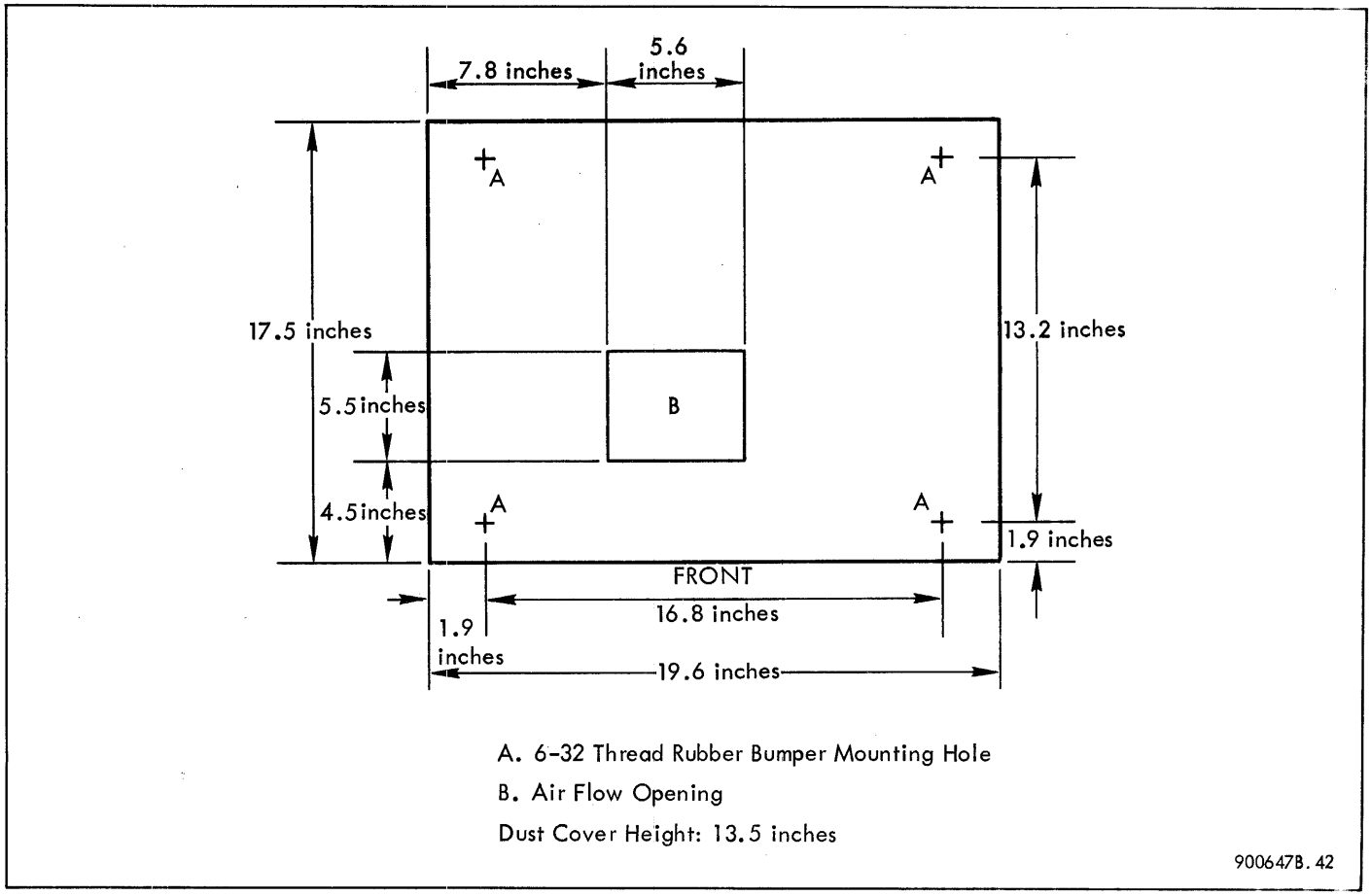


Figure 4-2. Model 9402 Dust Cover Housing Dimensions (Top View)

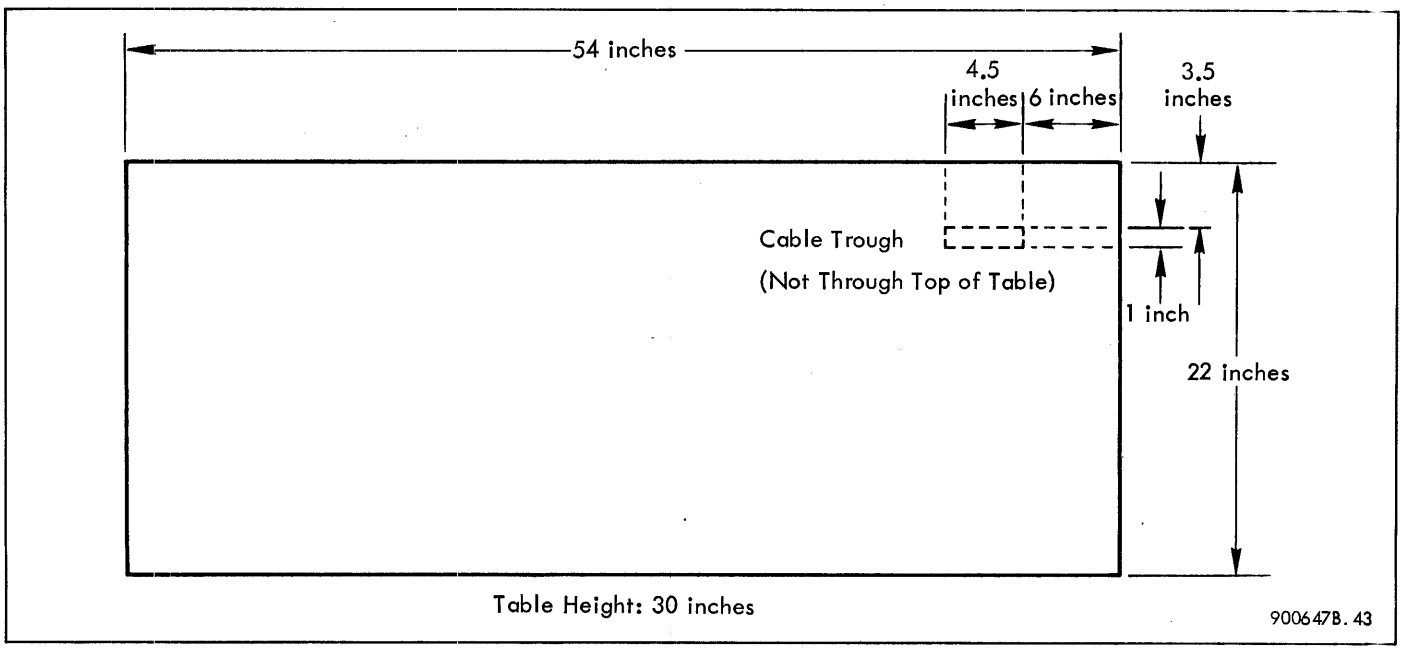


Figure 4-3. Model 92360 Table Dimensions (Top View)

are tagged according to voltage requirements. Cable lengths and part numbers are shown in table 4-4.

h. Connect 9448 dc power cable wires to appropriate computer power buses as indicated in table 4-5. The wires are tagged according to voltage requirements. The cable is 5 feet long.

i. Connect 9446 ac power plug P1 to an ac power source.

Table 4-3. Model 9446 DC Power Cable Connections

Wire No.	From Model 9446	To Power Supply
1	TB4-E-1	+50v dc
2	TB4-E-2	+25v dc
3	TB4-E-3	-25v dc
4	TB4-E-4	+ 8v dc
5	TB4-E-5	0v
6	TB4-E-6	Ground No. 1
7	TB4-E-7	Ground No. 2

Table 4-4. Model 9446 DC Power Cables

Length (ft)	Part No.
20 (std)	110951
10	113986
5	113839

Table 4-5. Model 9448 DC Power Cable Connections

Wire No.	From Model 9448	To Power Supply
1	A03 J45-E-47	+25v dc
2	A03 J45-E-46	-25v dc
3	A03 J45-E-45	+ 8v dc
4	A03 J45-E-44	0v

4-14 INITIAL CHECKOUT

4-15 Initial checkout of the MAGPAK tape system involves checking to see that all electromechanical functions are operable. Final mechanical adjustments of MAGPAK are

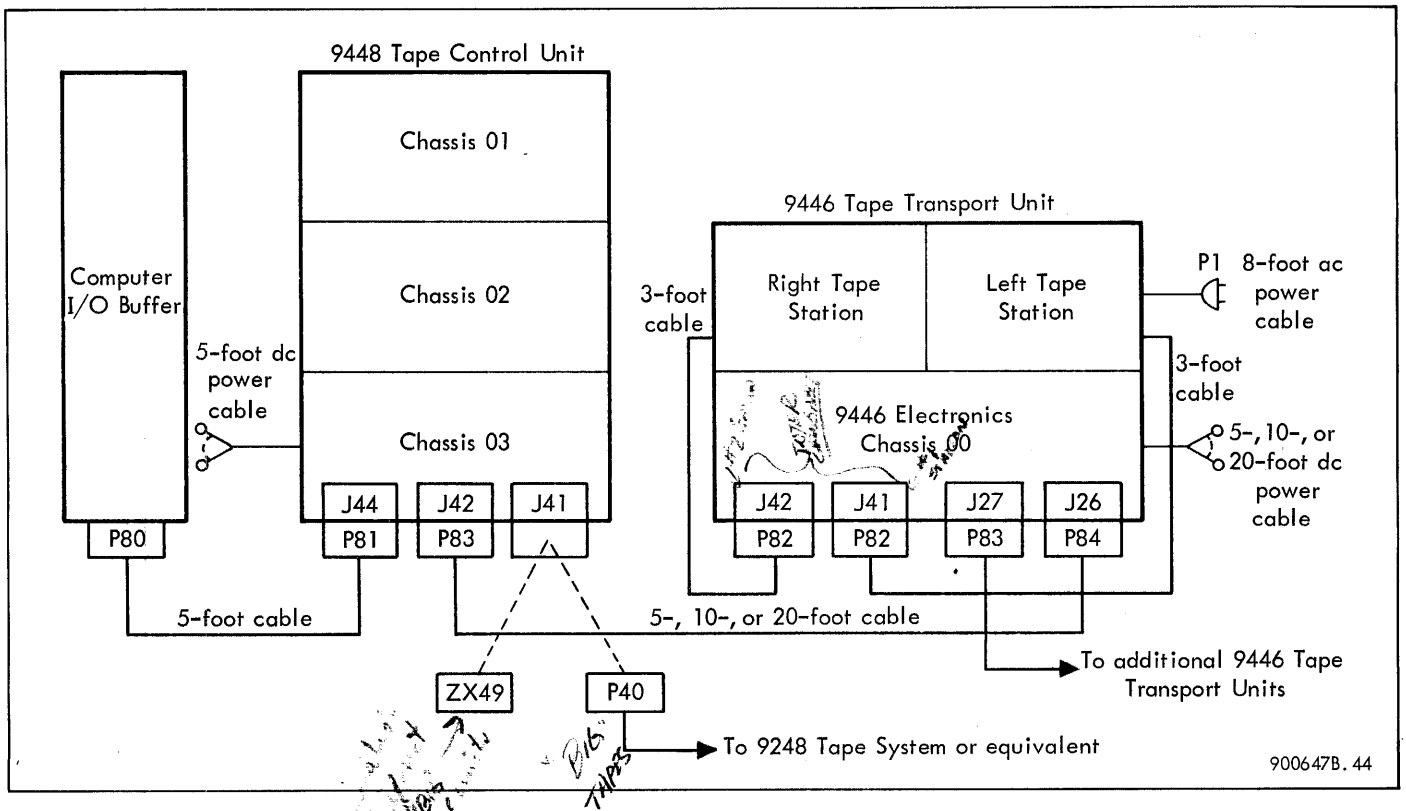


Figure 4-4. MAGPAK Interconnecting Cabling

made at the factory and should not have to be made again unless a part is replaced.

4-16 Initial checkout of MAGPAK is accomplished as follows: Apply power to the equipment and place the AUTO-MANUAL switch in MANUAL. Before loading tape cartridges on the transports, check to ensure that the capstans are rotating and the tension arms are in the correct position. Check to see that the reel motor hubs rotate when the FORWARD, REVERSE, and REWIND buttons are pressed. Note that right hub will not rotate in rewind. Also check the operation of the indicator lights.

4-17 Next, place tape cartridges on the transports and check to see that the tape is guiding correctly. Then check to determine if the beginning-of-tape and end-of-tape signals are working properly.

4-18 Operation of the system in the automatic mode can be checked by executing single-instruction EOM's for the desired operations, such as Read, Write, Scan, and Rewind. The status lines can be checked with appropriate SKS instructions, or by maintaining the unit in the addressed state.

4-19 If any of the above checks are unsatisfactory, perform the adjustment described under paragraph 4-30.

4-20 DIAGNOSTIC AND TEST ROUTINES

4-21 The operating status of the unit can be further checked by running a diagnostic or test routine. The following SDS Program Library routines are available:

a. Multi-Unit Magnetic Tape Exerciser (Catalog No. 044004).

b. 42-Kc Magnetic Tape Test Program, W-Buffer (Catalog No. 074001).

c. 42-Kc Magnetic Tape System Exerciser, W-Buffer (Catalog No. 074003).

4-22 Margin testing can be accomplished with other clock crystals or with an audio oscillator. The standard clock crystal (126 kc) is removed from the CX13 module, which is in location J26, chassis 03 of the tape control unit. Another crystal is plugged in on the module, or the audio oscillator is connected from 03-J26-E-32 to ground. Frequencies above 135 kc require a jumper from 01-J32-E-27 to ground (on the GK51 module) to defeat the speed test error. The transports normally operate at ±15% speed variation. This may be tried by writing at 108 kc to 145 kc, and reading at 126 kc.

4-23 MAINTENANCE

4-24 PREVENTIVE MAINTENANCE

4-25 No periodic lubrication of the transports or periodic replacement of parts is required. However, it is important that the tape and transports be kept clean. The read/write heads and all tape guide surfaces should be cleaned with denatured alcohol or a commercial magnetic tape head cleaner at least once per 8-hour shift. Also, when the tape unit is in operation, the front cover door should remain closed.

4-26 Satisfactory performance also requires that SDS tape cartridges be used, since these are controlled to a much higher quality standard than are the conventional audio-type cartridges that are commercially available.

4-27 TROUBLESHOOTING

4-28 Table 4-6 lists the most frequent malfunctions encountered in MAGPAK. In order to troubleshoot MAGPAK, of course, the technician must understand how the equipment works (see section III), and must be able to distinguish between normal and abnormal operation. Otherwise he will have difficulty defining the problem. Refer to section V of this manual for schematics and to section VI for assembly drawings and parts information.

4-29 Normal signal levels for the MAGPAK Tape System are shown in table 4-7. Other signals in the system are at normal SDS logic levels; that is, 0v for binary zero, and +8v for binary one.

Table 4-6. MAGPAK Troubleshooting Chart

Symptom	Possible Cause	Remedy
1. Power failure	No power input.	Check power connections (see paragraph 4-12).
	Fuse F1 (2 amp) blown.	Replace fuse (see schematic).
2. Motion functions (forward, reverse, rewind) inoperative; no indicator lights.	BOR or EOR switches open (occasionally BOR opens in rewind due to the increased tape tension).	Check tension arm position; if normal, adjust switches S8 or S9 (see paragraph 4-55).
	Fault relay K2 defective.	Replace K2 (see schematic).

Table 4-6. MAGPAK Troubleshooting Chart (Cont.)

Symptom	Possible Cause	Remedy
3. Rewind motion inoperative; other motions normal.	Rewind relay K1 defective.	Replace K1 (see schematic).
4. Capstans do not rotate; RESET button has been pushed.	BOR or EOR switches open.	Check tension arm position; if normal, adjust switches S8 or S9 (see paragraph 4-55).
	Fault relay K2 defective.	Replace K2 (see schematic).
5. Tape guides improperly; tape binds; tape breaks; tape winds unevenly; tape spills out of reel.	Cartridge loaded incorrectly.	Reload cartridge; check cartridge fit against spring clips and positioning pins (see paragraphs 2-29 and 4-65).
	Tension arm pins out of alignment.	Adjust tension arm pins (see paragraph 4-62).
6. Oxide accumulates.	Worn read/write head.	Replace read/head (see schematic). (Note: Read/write heads are sometimes scratched by careless removal and replacement of cross-talk shields.)
	Rough surface in tape guide path.	Replace defective part.
7. Tape movement erratic.	Capstan/pressure-roller force incorrect.	Adjust capstan/pressure-roller force (see paragraph 4-43).
8. Tape start-stop times irregular.	Capstan/pressure-roller gap incorrect.	Adjust capstan/pressure-roller (see paragraph 4-41).
8. (Cont.)	Reel motor brakes out of adjustment.	Adjust reel motor brake armature gap (see paragraph 4-46).
9. Tape tension incorrect; rewind time too slow.	Reel motor stall torque out of adjustment.	Adjust reel motor stall torque (see paragraph 4-50).
	Reel brakes out of adjustment.	Adjust reel motor brake armature gap (see paragraph 4-46).
10. Incorrect rewind speed; tape passes BOT marker on rewind.	Right reel motor torque out of adjustment.	Adjust right reel motor torque (see paragraph 4-52).
11. Tension arm oscillates.	Dashpot out of adjustment.	Adjust dashpot (see paragraph 4-60).
12. Tape hangs up on tension arm pins when cartridge is loaded.	Tape tension arm retraction mechanism out of adjustment.	Adjust retraction mechanism (see paragraph 4-57).
13. BOT or EOT signal inoperative; BOT or EOT signals triggered incorrectly.	Photosense amplifier out of adjustment.	Adjust HX48 (see paragraph 4-34).
	Photosense head lamp defective.	Replace lamp DS6. Readjust HX48 (see paragraph 4-34).
14. Parity error.	Tape damaged or worn.	Replace tape cartridge.
	Read/write head defective.	Replace read/write head (see schematic).
15. Read error.	Data amplifier level control out of adjustment.	Adjust HX29 (see paragraph 4-31).

i. Tighten lower screw on solenoid mounting bracket. Be careful to ensure that solenoid does not move as screw is tightened.

j. Tighten upper screw on solenoid mounting bracket and remove thickness gauge.

4-46 Reel Motor Brake Armature Gap Adjustment

4-47 The reel motor brake gap is set to 0.003 inch ±0.001 inch at the factory and should require no further attention unless the brake or reel motor is replaced. If the reel motor brake armature gap requires setting, follow the steps listed below.

CAUTION

Extreme care must be taken to ensure that the brake armature diaphragm (shown in figure 4-8) is not damaged during adjustment. The armature should be moved on the motor shaft by grasping the armature hub and not the armature disc itself. Any significant force applied to the armature disc will permanently deform the diaphragm.

a. Measure gap with thickness gauge. It should be 0.003 inch ±0.001 inch.

b. If adjustment is required, loosen setscrew in brake armature hub and slide armature on motor shaft until correct gap is attained.

c. Retighten setscrew.

d. Remeasure gap to ensure that armature did not move when setscrew was tightened.

4-48 Reel Motor Brake Torque Adjustment

4-49 With the dc power supply set to 50 volts, the reel motor brake torque should be adjusted to 5 in. oz ±10% to ensure proper functioning. A torque gauge with a chuck or adapter capable of grasping the reel motor shaft is required for this adjustment. Perform the following steps:

a. Apply dc power only to MAGPAK. Remove ac power by either removing fuse F-1 or by unplugging ac line cord.

b. Set dc supply to 50 volts.

c. Remove tape cartridge if present.

d. Energize brakes by placing AUTO-MANUAL switch in MANUAL position and pressing RESET button.

e. Attach torque gauge to motor shaft.

Note

In most cases, the torque can be measured most easily at the rear motor shaft since this does not require the removal of the reel motor hubs.

f. Rotate wrench slowly clockwise until brake slips. Read the torque necessary to just keep the brake slipping. Repeat in counterclockwise direction. The average of these two readings is the measured brake torque.

g. Adjust slider on R-1 (left brake) or R-2 (right brake) until average torque read in step f above is 5 in. oz.

Note

The slider is jumpered to one end of the resistor; moving the slider toward this end will decrease the brake torque.

4-50 Reel Motor Stall Torque Adjustment

4-51 Both the right and left reel motors should deliver a stall torque of 2.0 in. oz ±10% when the line voltage is 115 vac. The adjustment is made at the factory and should not have to be made again unless a motor is replaced. This adjustment requires a torque gauge with a chuck or adapter capable of grasping the reel motor shaft. See figure 4-9 and perform the following steps:

a. Apply power to MAGPAK.

b. Measure ac line voltage.

c. Remove cartridge if present.

d. Move load lever to RUN position and AUTO-MANUAL switch to MANUAL.

e. Press RESET button.

f. Attach torque gauge to reel motor shaft.

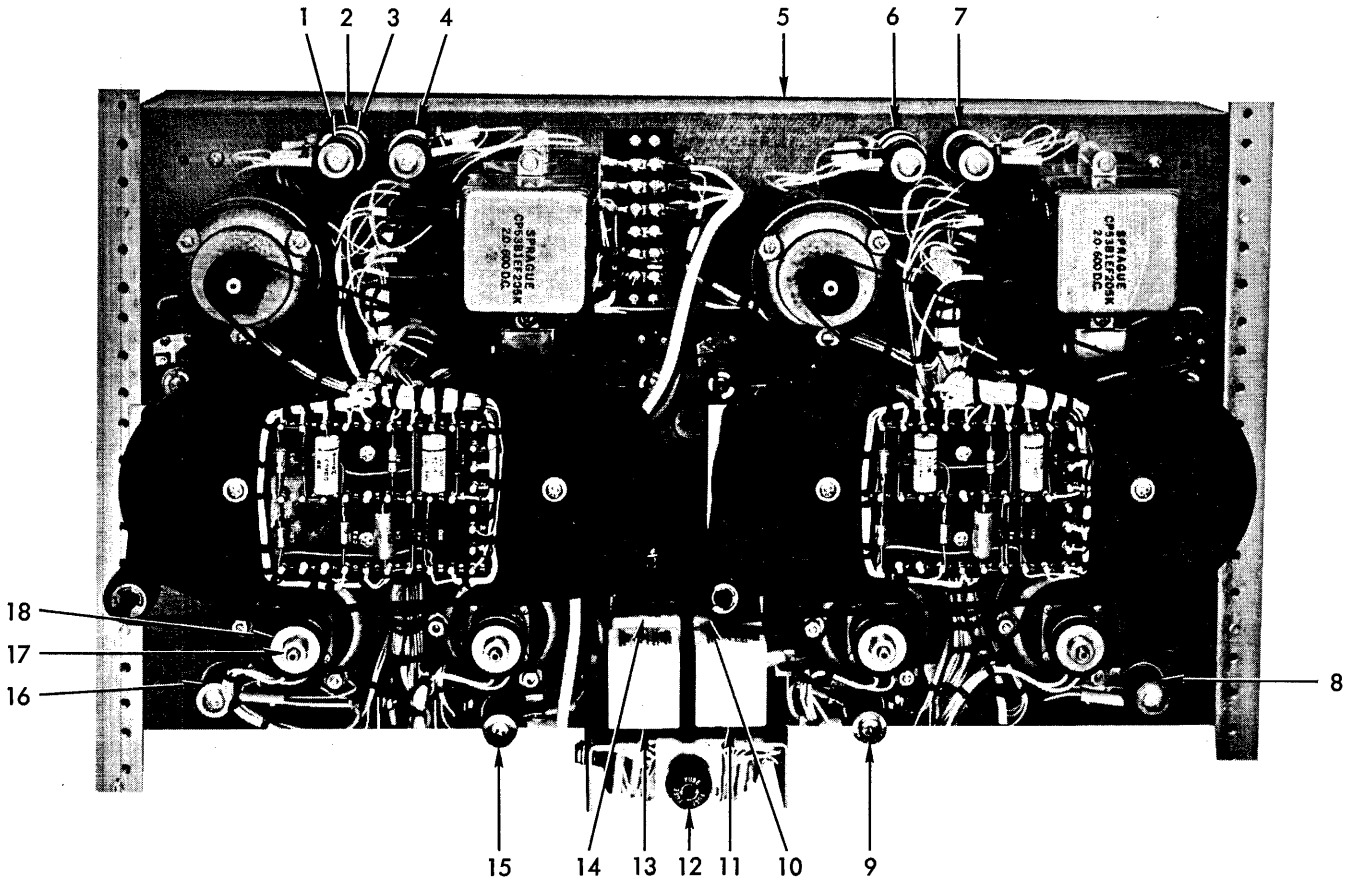
Note

It will usually be easier to measure the torque at the rear motor shaft since this does not require removal of reel motor hubs.

g. Press either FORWARD or REVERSE button on control panel to release reel motor brakes.

CAUTION

Care should be taken to ensure that the torque is applied gradually to the torque guage by holding the motor at stall with one hand and then releasing slowly, allowing the torque to build up. If this is not done, a spring-mass oscillation may build up between the torque gauge and the motor.



1. Slider No. 1 (same on both sides)
2. Slider No. 2 (same on both sides)
3. Resistor R3-R
4. Resistor R4-R
5. Mounting Plate
6. Resistor R3-L
7. Resistor R4-L
8. Resistor R1-L
9. Resistor R2-L
10. Relay K1-L
11. Relay K2-L
12. Fuse F1
13. Relay K2-R
14. Relay K1-R
15. Resistor R1-R
16. Resistor R2-R
17. Brake Armature Hub (same on all four units)
18. Brake Armature Diaphragm (same on all four units)

900647B.48

Figure 4-8. Model 9446 Tape Transport Mechanism

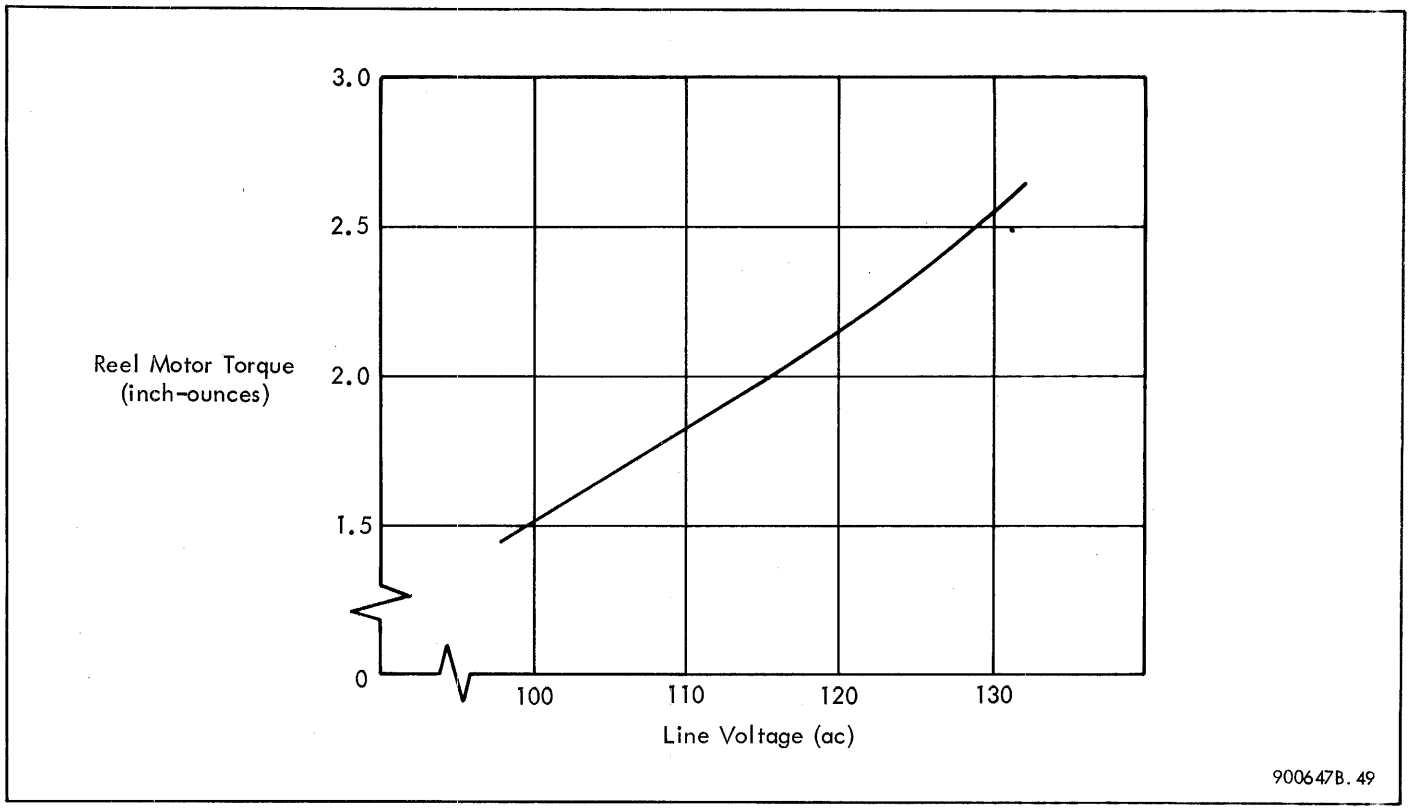


Figure 4-9. Reel Motor Stall Torque Adjustment

h. Allow motor to rotate very slowly in its normal direction and read torque gauge.

i. Refer to figure 4-3 to find correct torque for voltage measured in step b.

j. If torque is incorrect, remove power and reposition slider No. 1 on R-3 (right motor) or slider on R-4 (left motor). These sliders have a jumper wire connecting them to one end of the resistor; moving the slider toward this end of the resistor will decrease the torque.

k. Repeat steps h through j until proper torque is obtained.

4-52 Rewind Speed Adjustment

4-53 To ensure that the tape will stop with the BOT marker under the photosensor when rewinding, it is necessary to limit the tape speed as the end of rewind is approached. This is accomplished by varying the ac current through the main winding of the right reel motor (capacitor winding is opened by K1 during rewind), thereby changing the dynamic braking effect of the right motor. Linear tape speed should fall between 15 and 20 inches per second just before the BOT marker is reached. This range of speeds is manifested by a rotational speed range of 180 to 200 rpm at the right reel.

4-54 If it is necessary to adjust the rewind speed, perform the following steps:

a. Set input voltage to drive unit at 115 vac.

b. Load tape cartridge on transport.

c. Ensure that tape does not bind in cartridge.

d. Press REWIND button to initiate rewind.

e. Using a strobotac, measure rotational speed of right reel at time just prior to BOT marker entering the photosensor. This speed should be between 180 and 300 rpm. (If a strobotac is not available, observe the time required to rewind from EOT to BOT. It should be less than 2 minutes.

f. If speed is incorrect, remove power and adjust slider No. 2 (nearest mounting plate). To reduce speed move slider No. 2 toward slider No. 1. To increase speed, move slider No. 2 toward mounting plate.

g. Check to ensure tape stops with BOT marker under photosensor.

4-55 Tension Arm Limit Switch Adjustment

4-56 The tension arm limit switches (S8 and S9) should be adjusted to operate when the center-line of the tape tension

arm pickup pin is between the 1/16-inch limits, as measured from the edge of the tape cartridge web. See figure 4-10 and perform the following steps:

a. Place tape cartridge on MAGPAK.

b. Move load lever to RUN position.

c. Move tension arm pickup pin toward center of cartridge and note position of this pin when limit switch operates. Operation of switch will be manifested by an audible click of snap action mechanism.

Note

If environment is too noisy to hear the switch snap, use an ohmmeter across the switch contacts to detect operation.

d. If operational point is not between limits shown in figure 4-10, grasp switch actuator arm with a pair of long-nose pliers or a small soldering aid tool and bend it slightly, thereby changing operating point. Do not bend pickup pin.

e. Repeat steps c and d until switch operates at correct point.

4-57 Tension Arm Retraction Mechanism Adjustment

4-58 Proper adjustment of the retraction mechanism ensures that both tension arms retract far enough to prevent the tape from hanging up on the tension arm pin when a cartridge is placed on the transport.

4-59 There are two types of adjustment hardware. Some transports have an eccentric collar on the tension arm stop pin; other models have a link in the retraction mechanism which can be adjusted to proper length. Perform the following steps:

a. Place load-run lever in LOAD position.

b. Depending on type of adjustment hardware, either rotate eccentric or adjust length of link until both tension arms are fully retracted; i.e., stop pins of both arms bear against top of hole in transport casting.

4-60 Tension Arm Dashpot Adjustment

4-61 The tension arm dashpots should be adjusted as outlined below.

a. Place tape cartridge on transport with left reel full. Check to ensure that tension arms and reels do not bind in cartridge.

b. Program transport to run forward for 26 ms and stop for 26 ms alternately. This may be accomplished by using the start-stop program listed in table 4-8.

c. Adjust left tension arm dashpot by turning screw at bottom of tube until following two conditions are both met (note that turning screw clockwise increases damping):

1. Tension arm pin must move in at least 1/8 inch at the time the pressure roller engages. If not, damping is too high.

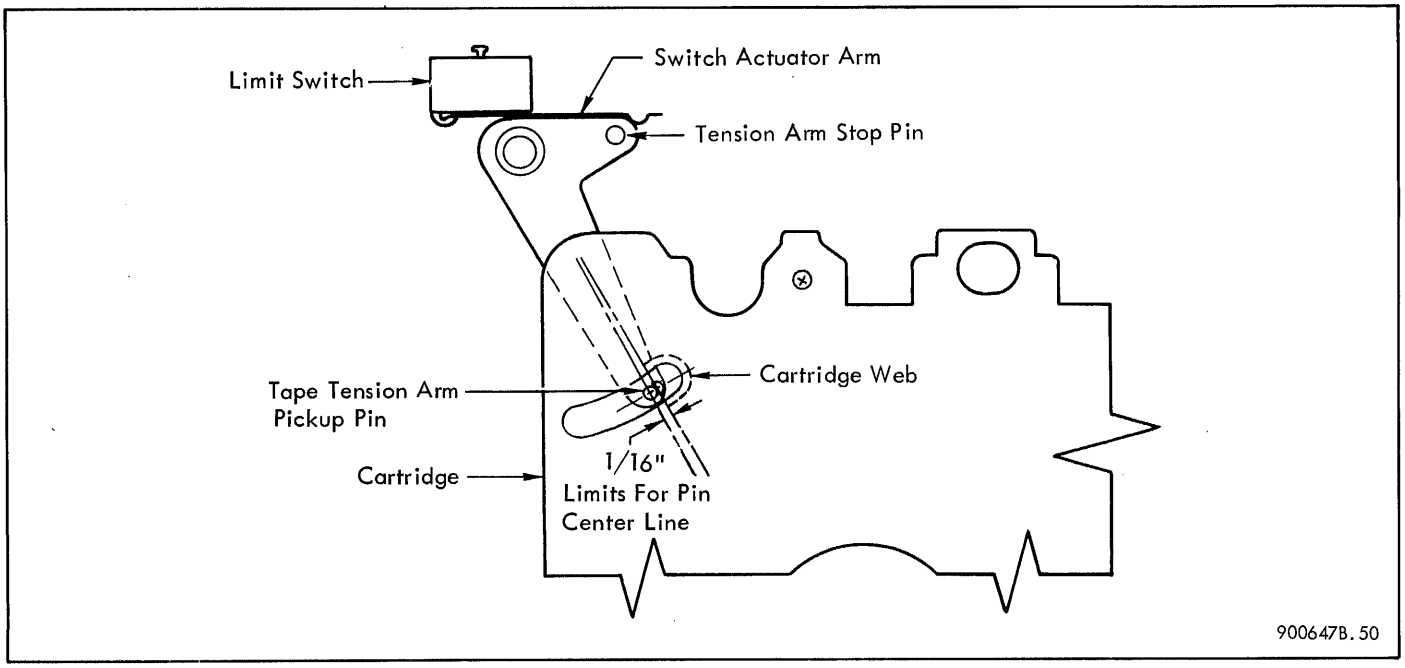


Figure 4-10. Tension Arm Limit Switch Adjustment

2. Arm should move out to "run" position and not bounce inward again; i.e., no oscillations. If the arm bounces or oscillates more than once, the damping is too low.

d. Repeat for right dashpot with tape alternately running reverse and stopping, and with right reel full.

4-62 Tension Arm Pickup Pin Adjustment

4-63 The tension arm pickup pin should be perpendicular to the center line of the tape path (that is, perpendicular to the transport casting surface) when under tension. If it is not, the tape is driven against the inside of the cartridge housing as it winds onto the reel. This eventually causes the reel to bind in the cartridge housing. This binding can occur when a cartridge wound on a poorly adjusted transport is run on another transport, regardless of whether the second transport is properly adjusted or not.

4-64 This adjustment is made at the factory and should not have to be made again unless the pin is accidentally bent. To make the adjustment, perform the following steps:

a. Place properly wound tape cartridge on transport.

b. Place AUTO-MANUAL switch in MANUAL and press FORWARD button.

c. Observe how tape passes over right tension arm pin as it winds onto right reel. Tape should be centered in cartridge housing as it travels over cartridge pin. There should be approximately 0.030 inch clearance between tape edge and cartridge housing on each side.

d. If tape is not centered, tension-arm pin should be adjusted by bending slightly. This is essentially a trial-and-error method which involves removing the cartridge, bending the pin, replacing the cartridge, and seeing how the tape runs over the pin. The pin is bent by inserting a 5/16-inch-diameter aluminum rod with a 1/8-inch hole over the pin and bending.

e. The adjustment procedure is the same for the left tension arm pin except that the tape must be run in the reverse direction to see how it winds onto the left reel.

f. Check rewind operation to ensure that tape winds onto left reel properly. If the pin is adjusted properly in step e above, tape should rewind in the center of the cartridge.

4-65 Tape Cartridge Fit Adjustments

4-66 In general, proper tape cartridge fit requires two conditions: first, the cartridge must be seated firmly on the transport; second, the cartridge reel must be located correctly with relation to the cartridge housing. Both of these factors affect tape guiding across the read/write head and tape winding on the reels. Incorrect cartridge fit results in tape buckling at the edges, binding, winding unevenly, etc. Refer to section II of this manual for instructions on cartridge loading procedure.

4-67 Cartridge Seating. The tape cartridge is held firmly in place by two spring clips which hold the sides of the cartridge, two locator pads on the transport casting, and a nylon hold-down button, the shaft of which slides into a notch at the bottom center of the tape cartridge. In addition, two positioning pins at the bottom of the transport casting serve as loading locations. If these pins are too low, the tape will bind between the top of the cartridge and the head guides. If they are too high, the cartridge cannot be loaded. When the cartridge is loaded on the transport, there should be a 0.005-inch to 0.020-inch clearance (depending on cartridge tolerances) between the bottom of the cartridge and the positioning pins. The positioning pins are adjusted by bending them up or down.

4-68 If a tape cartridge adjustment fixture (SDS part No. 126603) is available, the positioning pins can be adjusted as follows:

a. Place adjustment fixture on transport.

b. Tighten two nylon screws on top of adjustment fixture against head guide pins so that fixture is locked in place.

c. Insert a 0.007-inch thickness gauge between positioning pins and bottom of adjustment fixture.

d. Bend pins up or down until a slight resistance to the movement of the thickness gauge is felt.

e. Loosen plastic screws and remove adjustment fixture.

4-69 Cartridge Reel Location. The cartridge reels should turn freely in the cartridge housing. In order to do so, the reel motor hubs should pick up the cartridge reels and center them in the plane of the cartridge housing so that there is approximately 0.030 inch between each inside surface of the cartridge housing and the edge of the tape. Also, the reel motor hubs should not touch the cartridge housing or scrape against it as they rotate.

4-70 The front surface of the reel motor hubs should be a distance of 0.207 inch ±0.005 inch above the locator pads and hold-down button base (which are on the same plane). This adjustment is made at the factory and should not have to be made again unless a part is replaced. A special adjustment fixture (SDS part No. 126603 is required to set the reel motor hub height correctly. See figure 4-11 and perform the following steps:

a. Place adjustment fixture on transport.

b. Tighten two nylon screws at top of fixture against head guide pins so that fixture is locked in place.

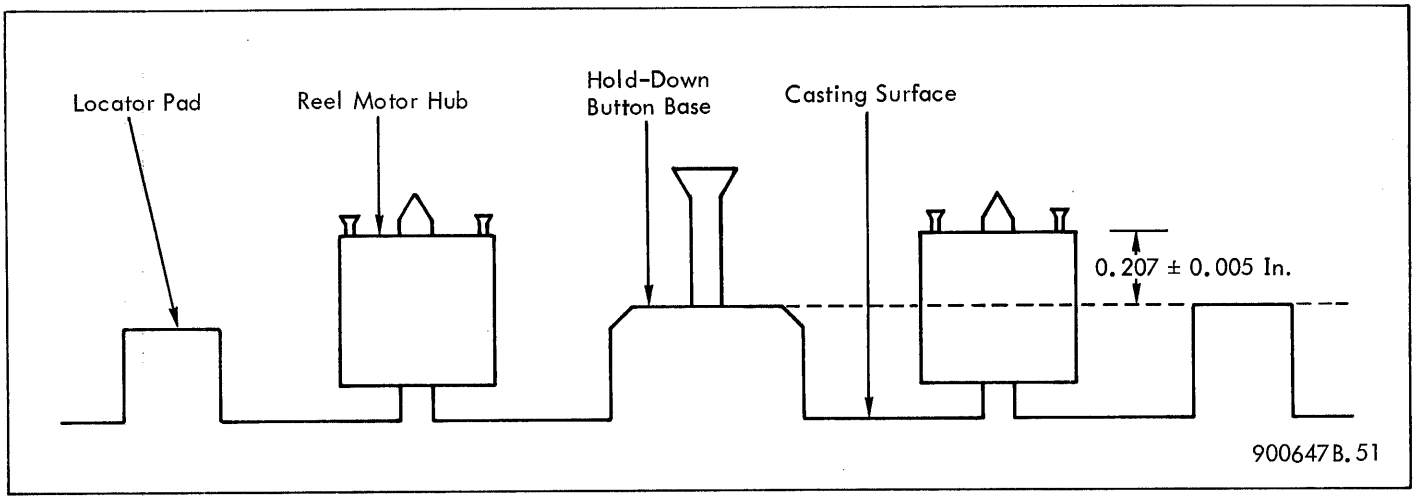


Figure 4-11. Reel Motor Hub Location (Top View)

c. Loosen reel motor hub setscrews.

d. Slide hubs out until they contact recessed groove of fixture.

e. Retighten setscrews.

4-71 FINAL CHECKOUT

4-72 Final checkout of the over-all mechanical performance of the MAGPAK transport can be accomplished using the "satellite" (signal noise) test described below. This test allows the operator to detect marginal mechanical performance of the unit and make any necessary adjustments.

4-73 The satellite test consists of a program which records continuous ones on a reel of tape and then reads these ones back in a program-controlled start-stop sequence. The transport alternately runs forward (or reverse) for 26 milliseconds and then stops for 26 ms. The wave-envelope and gap of the read signals are displayed on an oscilloscope and observed by the operator. If the test is not satisfactory, the proper adjustment is made and the test is rerun. (Note that read/write error indications during this test should be disregarded. These indications may occur because of the "illegal" programming methods used to achieve fast start-stop timing.)

4-74 The desired read signal shape is shown in figure 4-12. The wave-envelope should be even (not broken up) and there should be no satellites (noise) in the gap. Figure 4-13 shows satellites in the gap; figure 4-14 shows an uneven wave-envelope. A common cause of satellites is misalignment of the tension-arm dashpot; a common cause of an uneven envelope is improper skew (due to capstan/pressure-roller misalignment). These are the most common causes of an undesirable read-back signal shape. However, other mechanical functions (motor torque, brakes, etc.) may be responsible.

4-75 The satellite test uses the program listed in table 4-8. Figure 4-15 is a flow chart of the program. To run the test, perform the following steps:

a. Load tape cartridges on both MAGPAK tape stations.

b. Load program into computer.

c. Reset BP-1 and start program by entering memory location 200_8. Program will not write continuous ones.

d. After recording an ample amount of tape (about 1/3 of a reel), set BP-1. This will rewind tape and begin read start-stop sequence in forward direction.

e. Connect oscilloscope to J44 pin 40. Synchronize on J39 pin 42. Compare waveform observed with figure 4-12.

f. To check tape motion in reverse direction, set BP-2. Change synchronize point to J39 pin 35.

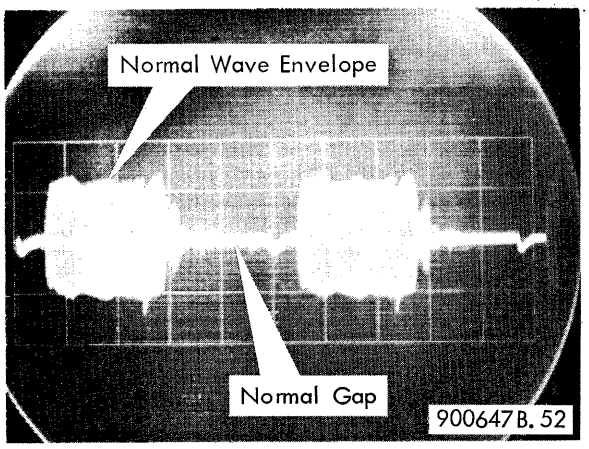


Figure 4-12. Read Signal Normal Wave Envelope

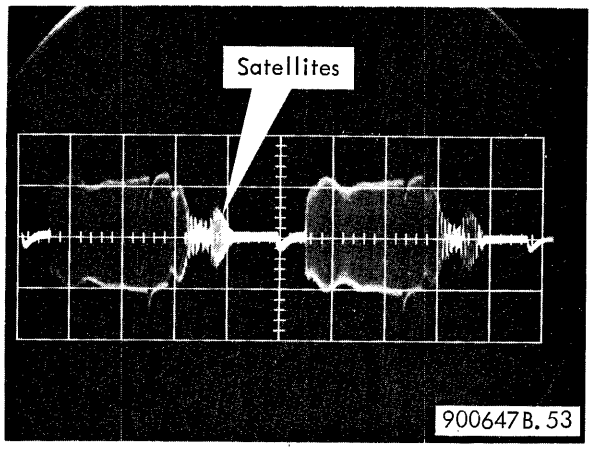


Figure 4-13. Read Signal Gap Noise

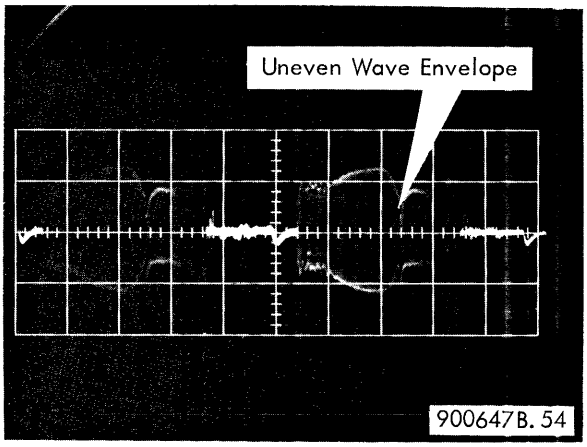


Figure 4-14. Read Signal Uneven Wave Envelope

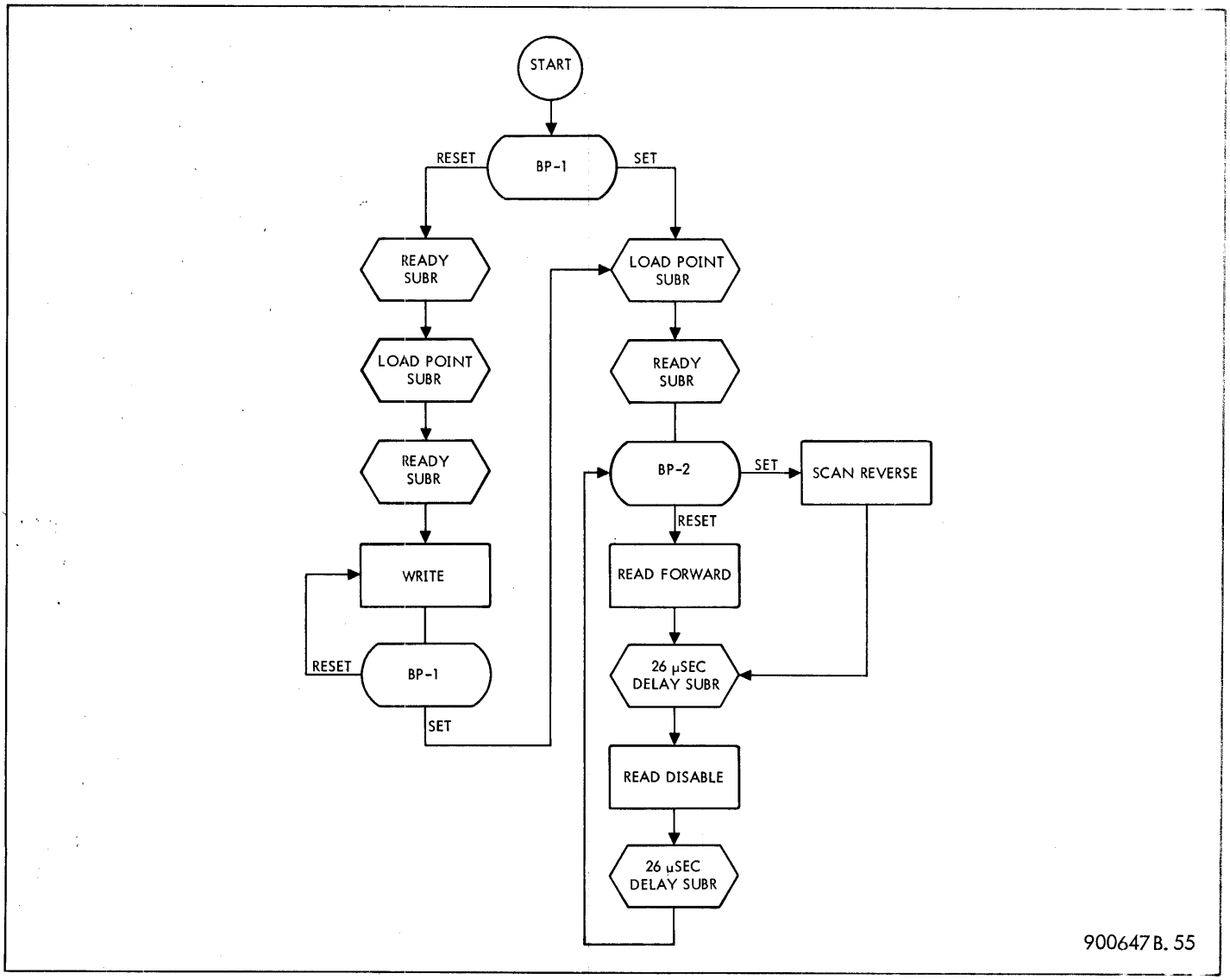


Figure 4-15. Satellite Test Program Flow Chart

Table 4-8. Satellite Test Program

Memory Location	Instruction Code (Octal)	Instruction Mnemonic	Remarks
		INITIALIZE	
200	0 40 20400	BPT1	Breakpoint 1 set?
201	0 01 00217	BRU	Yes; branch to read test
202	0 43 00227	BRM	No; mark place and branch to ready subroutine
203	0 43 00235	BRM	Mark place and branch to load-point subroutine
204	0 43 00227	BRM	Mark place and branch to ready subroutine
		WRITE DATA	
205	0 02 0365n	WTB	Write tape in binary; unit n
206	0 12 00212	MIW	Memory into W-buffer when empty
207	0 40 20400	BPT1	Breakpoint 1 set?
210	0 01 00217	BRU	Yes; branch to read test
211	0 01 00206	BRU	No; branch to MIW write constant
212	7 77 77777		Write constant (all ones)
213	0 00 00000		Write constant (all zeroes)?
214	0 51 00242	BRR	Return branch for delay subroutine
		SCAN REVERSE	
215	0 02 0763n	SRB	Scan reverse in binary; unit n
216	0 01 00224		Branch to BRM-delay subroutine

Table 4-8. Satellite Test Program (Cont.)

Memory Location	Instruction Code (Octal)	Instruction Mnemonic	Remarks
		READ TEST	
217	0 43 00235	BRM	Mark place and branch to load-point subroutine
220	0 43 00227	BRM	Mark place and branch to ready subroutine
221	0 40 20200	BPT2	Breakpoint 2 set?
222	0 01 00215	BRU	Yes; branch to scan reverse in binary
		READ FORWARD	
223	0 02 0361n	RTB	No; read tape in binary; unit n
224	0 43 00242	BRM	Mark place and branch to delay subroutine
		DISABLE READ	
225	0 02 00601	RKB	Read keyboard
226	0 01 00247	BRU	Branch to re-start delay
		READY SUBROUTINE	
227	0 00 00000		Branch return
230	0 40 21000	BRTW	W-buffer ready?
231	0 01 00230	BRU	No; branch to ready test
232	0 40 1041n	TRT	Yes; tape ready test; unit n
233	0 51 00227	BRR	Tape ready; return branch
234	0 01 00232	BRU	Tape not ready; branch to tape ready test
		LOAD POINT SUBROUTINE	
235	0 00 00000	BRM	BRM return

Table 4-8. Satellite Test Program (Cont.)

Memory Location	Instruction Code (Octal)	Instruction Mnemonic	Remarks
236	0 02 1401n	REW	Rewind; unit n
237	0 40 1201n	BTT	Beginning of tape?
240	0 51 00235	BRR	Yes; return branch
241	0 01 00237	BRU	No; branch to BTT
DELAY SUBROUTINE			
242	0 00 00000		BRM return
243	0 71 00246	LDX	Load Index Register with delay constant
244	0 41 00214	BRX	Increment Index Register and branch

Table 4-8. Satellite Test Program (Cont.)

Memory Location	Instruction Code (Octal)	Instruction Mnemonic	Remarks
245	0 01 00244	BRU	Branch to BRX
246	0 00 35500 or 0 00 27000		Delay constant for 910/920 Computers Delay constant for 925/930/9300 Computers
RESTART DELAY			
247	0 43 00242	BRM	Mark place and branch to delay subroutine
250	0 01 00221	BRU	Branch to BP-2 read test

SECTION V
PARTS LIST

5-1 GENERAL

5-2 This section contains tables listing the replaceable parts for the MAGPAK Tape System. Only those parts recommended for replacement in the field are listed. Each table is accompanied by one or more illustrations showing the locations of the parts.

5-3 In each table, parts are listed in alphabetical order, and indentions are used in the DESCRIPTION column to show parts relationship. Parts manufacturers are listed in each table by supplier code number. The name and address of the manufacturer can be found from the code number by using the supplier code index in table 5-21.

Table 5-1. Model 9446 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-1-	Assembly, Model 9446		SDS	107636	
55	. Block, terminal molded barrier	TB3-L, TB3-R	51		2
35	. Brake, magnetic, 28vdc	L1-L, L1-R L2-L, L2-R	160	FB-090	4
5-2	. Cable assembly, plug module	P82	SDS	107805	2
	. . Diode, SDS 103	CR1-CR11	4, 12, 13, 14	1N914A	22
	. . Resistor, 3.9k, 2%, 1/2w	R5, R6	36, 38, 73		4
5-3	. Cable assembly, plug module	P83-P84	SDS	107806	1
	. . Capacitor, tantalum, 100 µf, 20%, 20v	C1, C2	26, 27, 74		2
	. . Capacitor, mylar, 0.0047 µf, 20%, 20v	C3, C4	26, 27, 74		2
	. . Diode, SDS 103	CR1-CR7	4, 12, 13, 14	1N914A	7
	. . Diode, Zener, SDS 108	CR8, CR9	13, 15, 28	1N964A	2
	. . Inductor, molded, 10 µh, 5%	L1, CR1-CR7	49, 90, 91		16
	. . Resistor, 47 ohm, 2%, 1/2w	P84R1, P83R1-R15	36, 38, 73		16
	. Capacitor, oil impregnated, 2 µf, 20%	C1L-C3L, C1R-C3R	80, 81		6
	. Capacitor, tantalum, 15 µf, 20%, 50v	C4L-C6L C4R-C6R	22, 23, 77		6
	. Capacitor, mylar, 0.15 µf, 10%	C7L, C7R C8L, C8R	26, 27, 74		4
	. Capacitor, oil impregnated, 0.25 µf, 20%	C9L, C9R	80, 81		2
	. Connector, soldertail, 47 pin	J26-J45	82		20
	. Diode, SDS 113	CR1L-CR3L, CR1R-CR3R	26, 30, 68	1N189	6
	. Fuse, 3AG, 2 amp, 250v	F1	48		1
	. Head, stack, magnetic tape, SDS 106722		166, 167		2
	. Lamp, miniature incandescent	DS1L-DS5L, DS1R-DS5R	163	CF03	10

Table 5-1. Model 9446 Replaceable Parts (Cont.)

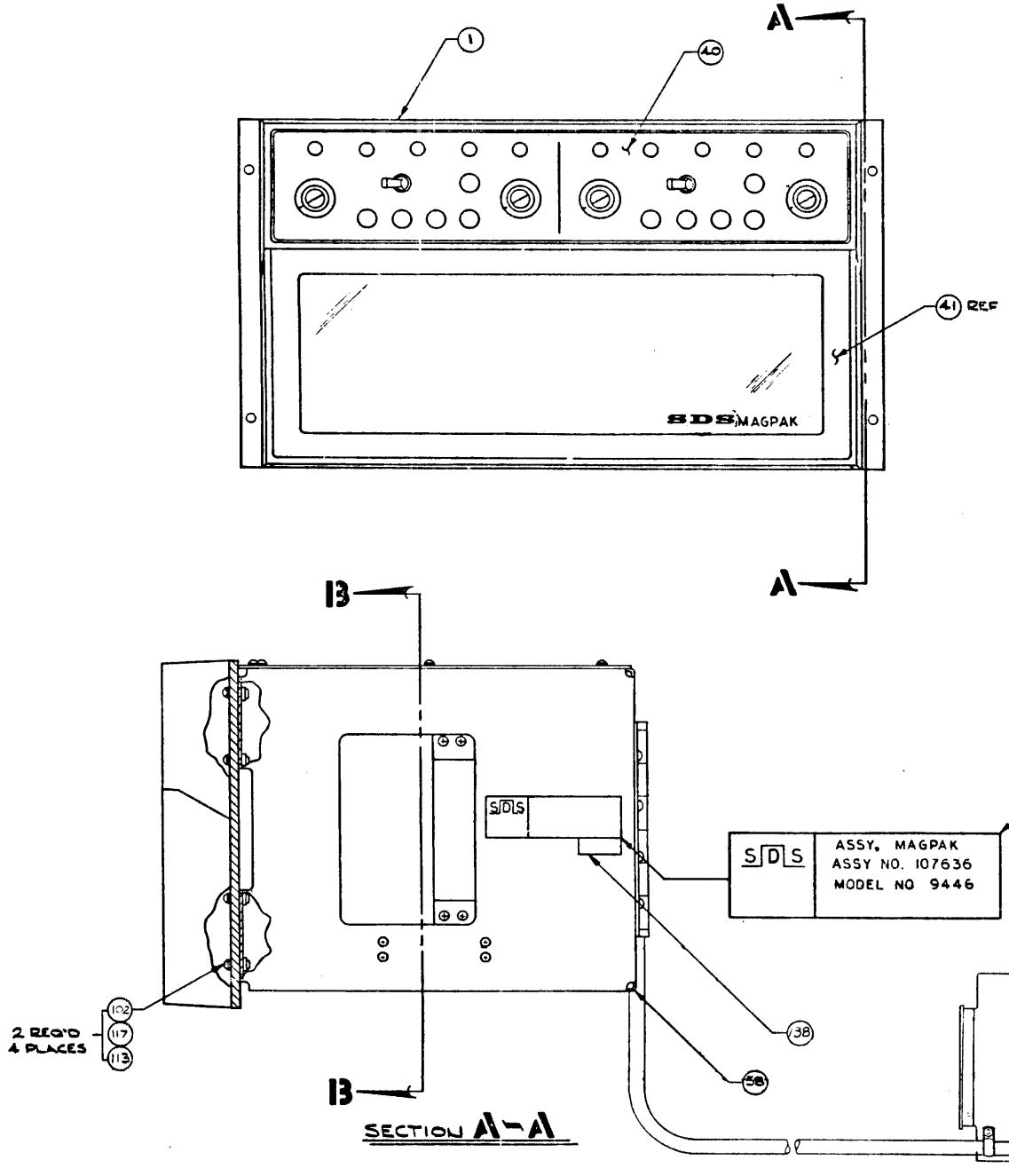
Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
	. Lamp, incandescent	DS6L, DS6R	84	253	2
5-1	. Module, Cable Driver AX14 (See table 5-3 for replaceable parts)		SDS	102853	2
5-1	. Module, DC Flip-Flop FH19 (See table 5-6 for replaceable parts)		SDS	103134	1
5-1	. Module, Diode Gate GK51 (See table 5-10 for replaceable parts)		SDS	100246	4
5-1	. Module, Data Amplifier HX29 (See table 5-11 for replaceable parts)		SDS	103387	1
5-1	. Module, Read Amplifier HX30 (See table 5-12 for replaceable parts)		SDS	103370	1
5-1	. Module, Gate Write Ampl HX31 (See table 5-13 for replaceable parts)		SDS	107429	1
5-1	. Module, Photo Sense Ampl HX48 (See table 5-14 for replaceable parts)		SDS	117696	1
5-1	. Module, AND/OR Inverter IH10 (See table 5-15 for replaceable parts)		SDS	100137	1
5-1	. Module, Inverter Amplifier IK51 (See table 5-18 for replaceable parts)		SDS	100388	2
5-1	. Module, Relay Driver RK53 (See table 5-19 for replaceable parts)		SDS	100905	2
5-1-5	. Motor, capstan drive, SDS 107650	M1L, M1R	165		2
5-1-6	. Motor, reel, SDS 107225	M2L, M2R	165		2
	. Post, extractor, fuse	XF1	48, 49	HPK-N-342002	1
	. Relay, 24 vdc	K1L, K1R, K2L, K2R	164	KHP-17D11	4
5-1-68	. Resistor, variable, 2k, 10%	R1L, R1R, R2L, R2R	45, 100		4
5-1-60	. Resistor, variable, 500 ohm, 10%	R3L, R4L, R3R, R4R	45, 100		4
	. Resistor, 22 ohm, 2%, 1/2w	R7L, R7R	36, 38, 73		2
	. Resistor, 12k, 2%, 1/2w	R8L, R8R	36, 38, 73		2
	. Resistor, 47 ohm, 2%, 1/2w	R9L, R9R R10L, R10R	36, 38, 73		4
	. Resistor, 100 ohm, 2%, 25w	R11L, R12L, R11R, R12R	36, 38, 73		4
	. Resistor, 56 ohm, 2%, 1/2w	R131, R13R	36, 38, 73		2
	. Resistor, 82 ohm, 2%, 1/2w	R14L, R14R	36, 38, 73		2
	. Resistor, 1.2k, 2%, 1/2w	R15L, R15R	36, 38, 73		2
	. Socket, relay mounting	XK1L, XK1R, XK2L, XK2R	164	27E006	4

Table 5-1. Model 9446 Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-1-60	. Solenoid, 25 vdc	L3L, L3R, L4L, L4R	161	A-348-2	4
	. Switch, rotary, 12 position	S1L, S1R, S2L, S2R	55	PA-2001	4
	. Switch, toggle, dpdt	S3L, S3R	106	83054-SE	2
	. Switch, pushbutton	S4L-S7L S4R-S7R S13L, S13R	113	C113-P-3	10
	. Switch, spring action	S8L, S8R, S9L, S9R	162	1SM1	4
	. Switch, snap action	S10L, S10R S11L, S11R	162	V3	4
	. Transistor, silicon photo conductive	Q1L, Q1R, Q2L, Q2R	SDS	108272	4

MODULE LOCATION CHART

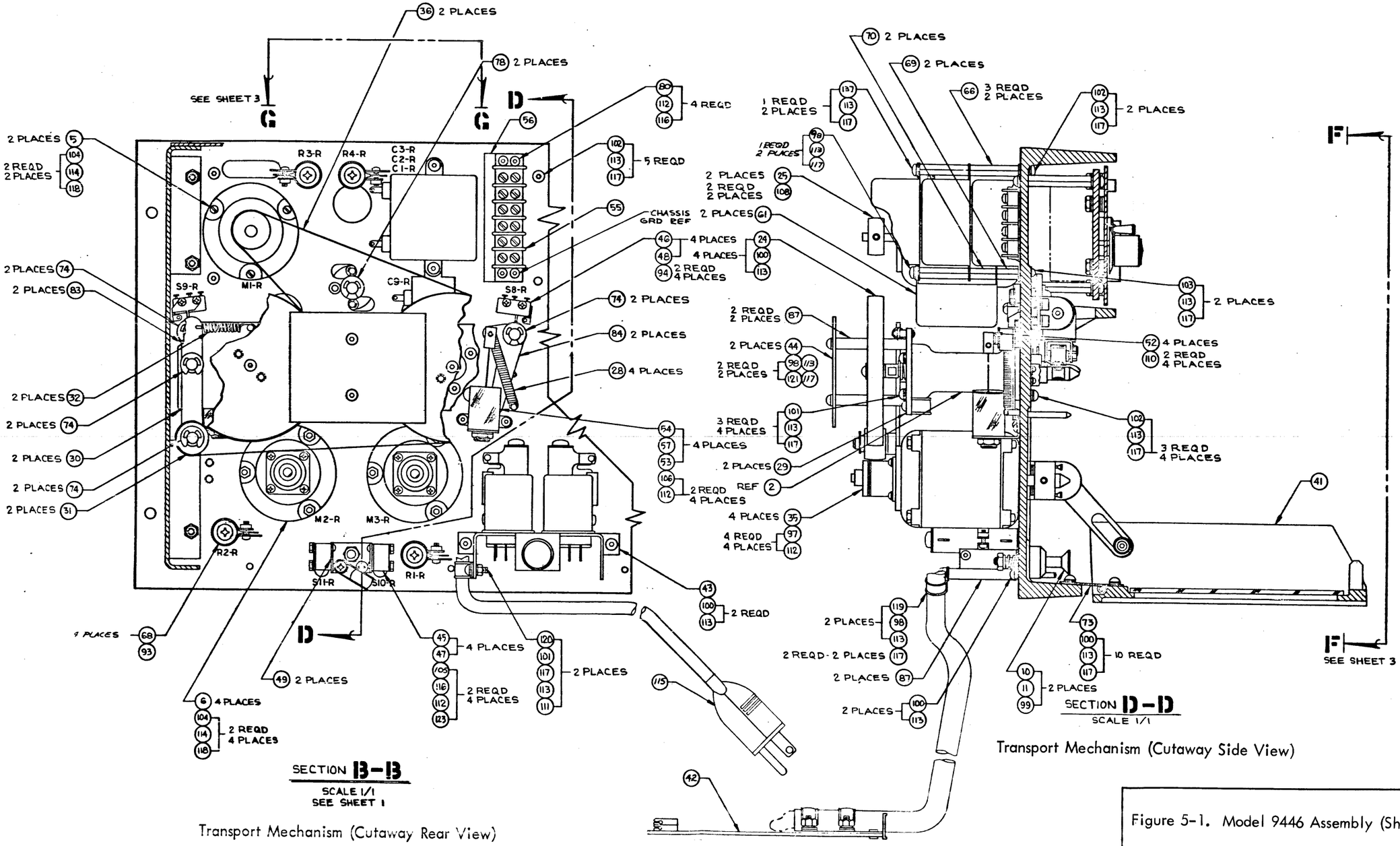
CHASSIS	LOCATION	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
00	TYPE	HX 30	HX 29	IH 10			IK 51	GK 51	HX 31	RK 53	AX 14	IK 51	GK 51	HX 48	FH 19	GK 51	GK 51	RK 53	AX 14		
	KEY	3 39	3 37	2 44	6 34	6 34	2 8	2 22	3 41	8 22	20 24	2 8	2 22	5 11	16 40	2 22	2 22	8 22	20 24	6 36	6 38



Front and Side Views

107636-1F

Figure 5-1. Model 9446 Assembly (Sheet 1 of 3)

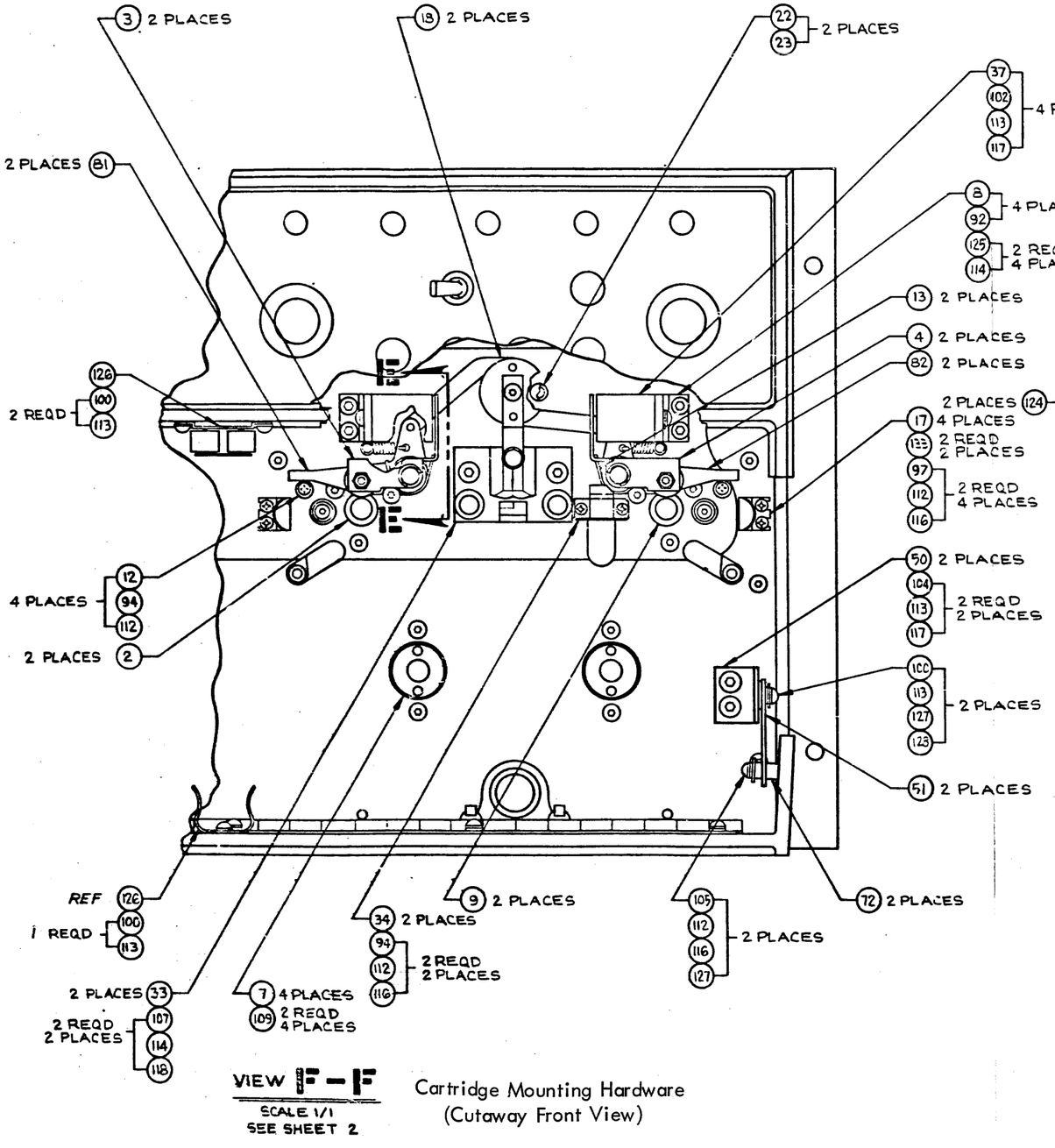


Transport Mechanism (Cutaway Rear View)

Transport Mechanism (Cutaway Side View)

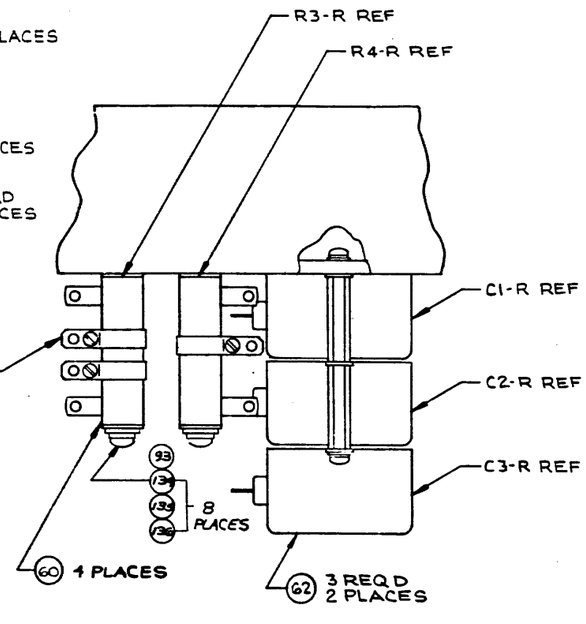
Figure 5-1. Model 9446 Assembly (Sheet 2 of 3)

107636-2F



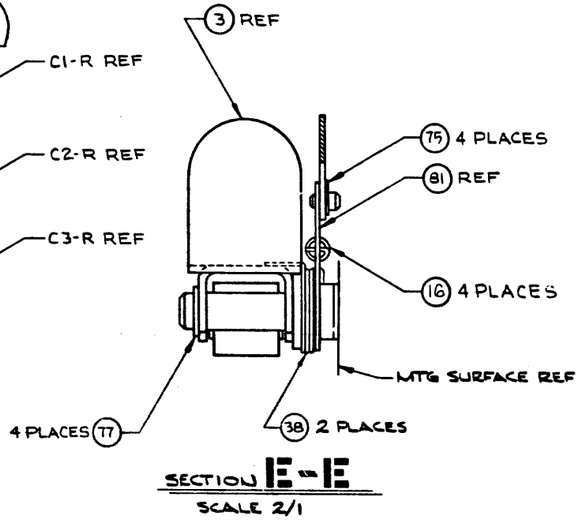
VIEW F-F
SCALE 1/1
SEE SHEET 2

Cartridge Mounting Hardware
(Cutaway Front View)



VIEW G-G
SCALE 1/1
SEE SHEET

Transport Mechanism Detail
(Cutaway Top View)

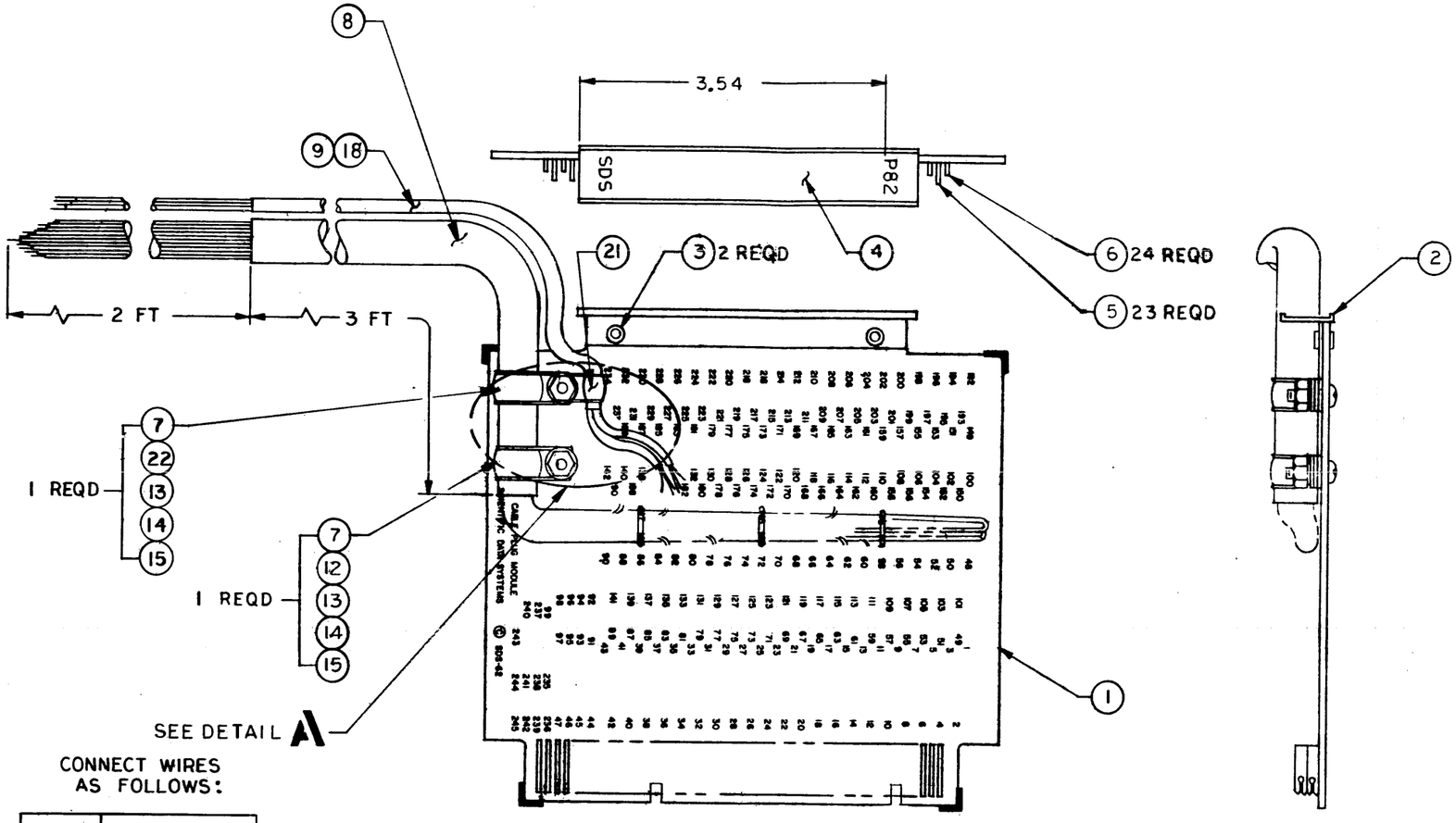


SECTION E-E
SCALE 2/1

Pressure Roller Assembly
(Side View)

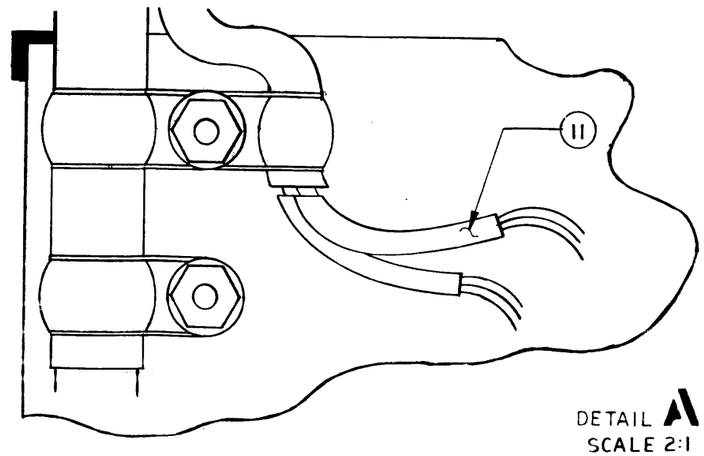
Figure 5-1. Model 9446 Assembly (Sheet 3 of 3)

107636-3F



CONNECT WIRES AS FOLLOWS:

ITEM NO	TO P82 –	
8	8, 9, 10, 92, 100 THRU 106 110, 112, 113 115 THRU 132 138, 139, 141, 142, 160	
9	BLK	133
	WHT	134
	SHLD	135
9	BLK	136
	WHT	137
	SHLD	135



DETAIL A
SCALE 2:1

Figure 5-2. Cable Plug Module P82 Assembly

107805-1G

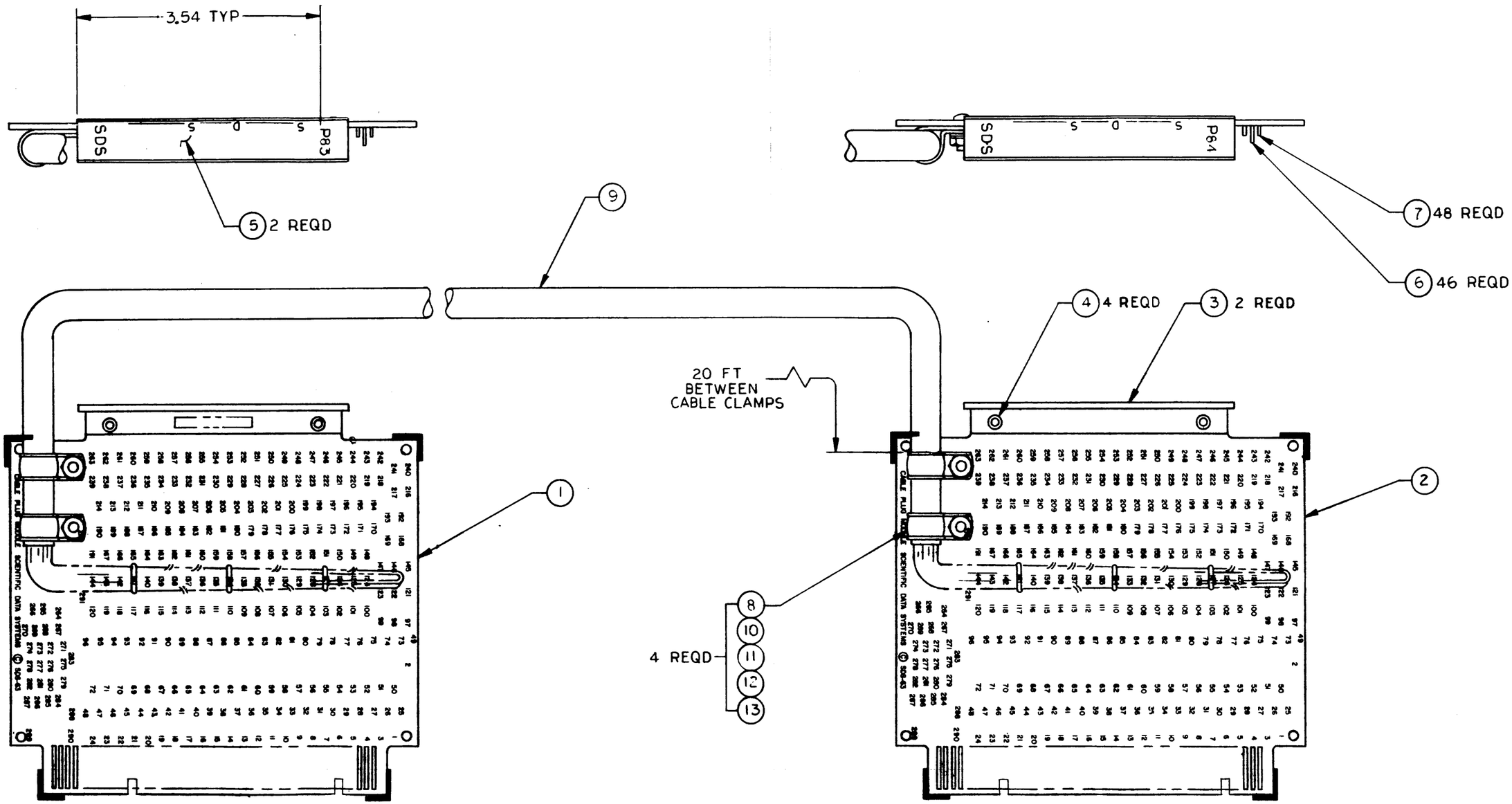
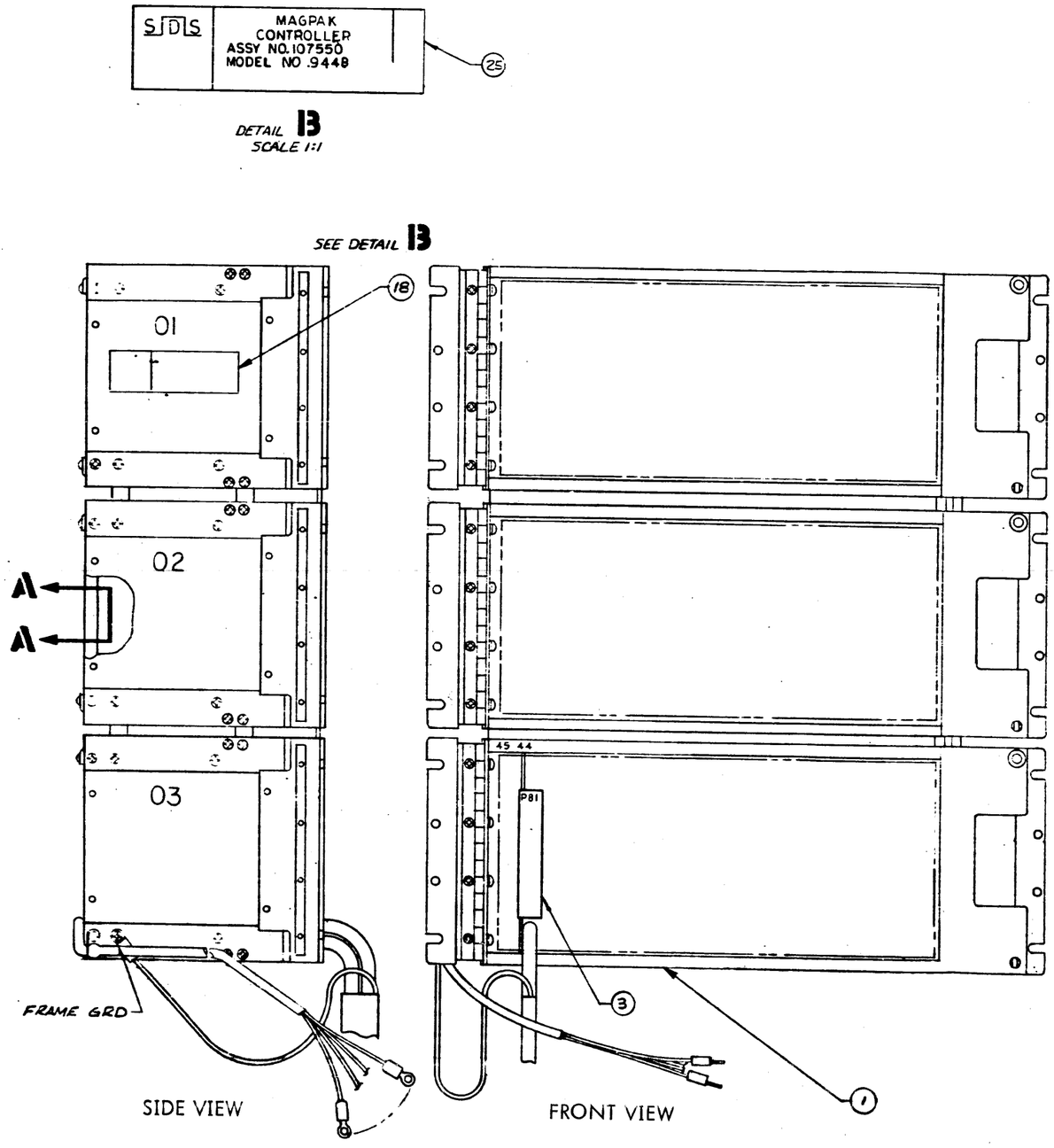


Figure 5-3. Cable Plug Module P83-P84 Assembly

107806-1H

Table 5-2. Model 9448 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-2)	Part No.	Qty
5-4	Assembly, Model 9448		SDS	107550	
5-5	. Cable assembly, plug module	P80-P81	SDS	107803	1
	. . Diode, SDS 103	P80CR1-CR4	4, 12, 13, 14	1N914A	4
	. . Inductor, molded, 100 μh, 5%	P80L1-L26	42, 90, 91		26
	. . Inductor, molded, 10 μh, 5%	P81L32-L36	42, 90, 91		5
	. . Resistor, 470 ohm, 2%, 1/2w	P80R1-R31	16, 17		31
	. . Resistor, 47 ohm, 2%, 1/2w	P81R32-R36	16, 17		5
5-4	. Connector, soldertail, 47 pin	01J26-J45 02J26-J45 03J26-J45	82	7008-47	60
5-4	. Module, Cable Driver AX14 (See table 5-3 for replaceable parts)		SDS	102853	4
5-4	. Module, Crystal Clock Generator CX13 (See table 5-4 for replaceable parts)		SDS	102171	1
5-4	. Module, Counter Flip-Flop FH15 (See table 5-5 for replaceable parts)		SDS	101026	8
5-4	. Module, DC Flip-Flop FH19 (See table 5-6 for replaceable parts)		SDS	103134	1
5-4	. Module, Gate Expander GH10 (See table 5-7 for replaceable parts)		SDS	100149	4
5-4	. Module, Gate Expander GH11 (See table 5-8 for replaceable parts)		SDS	101769	1
5-4	. Module, Gate Expander GH14 (See table 5-9 for replaceable parts)		SDS	104431	5
5-4	. Module, Diode Gate No. 1 GK51 (See table 5-10 for replaceable parts)		SDS	100246	4
5-4	. Module, AND/OR Inverter IH10 (See table 5-15 for replaceable parts)		SDS	100137	8
5-4	. Module, OR Gate Inverter IH11 (See table 5-16 for replaceable parts)		SDS	100319	2
5-4	. Module, AND Inverter IH12 (See table 5-17 for replaceable parts)		SDS	101767	9
5-4	. Module, Inverter Amplifier IK51 (See table 5-18 for replaceable parts)		SDS	100388	1
5-4	. Module, Digital-to-Staircase Converter SX58 (See table 5-20 for replaceable parts)		SDS	109413	1
5-4	. Module, Termination ZX49		SDS	111084	1



MODULE LOCATION CHART

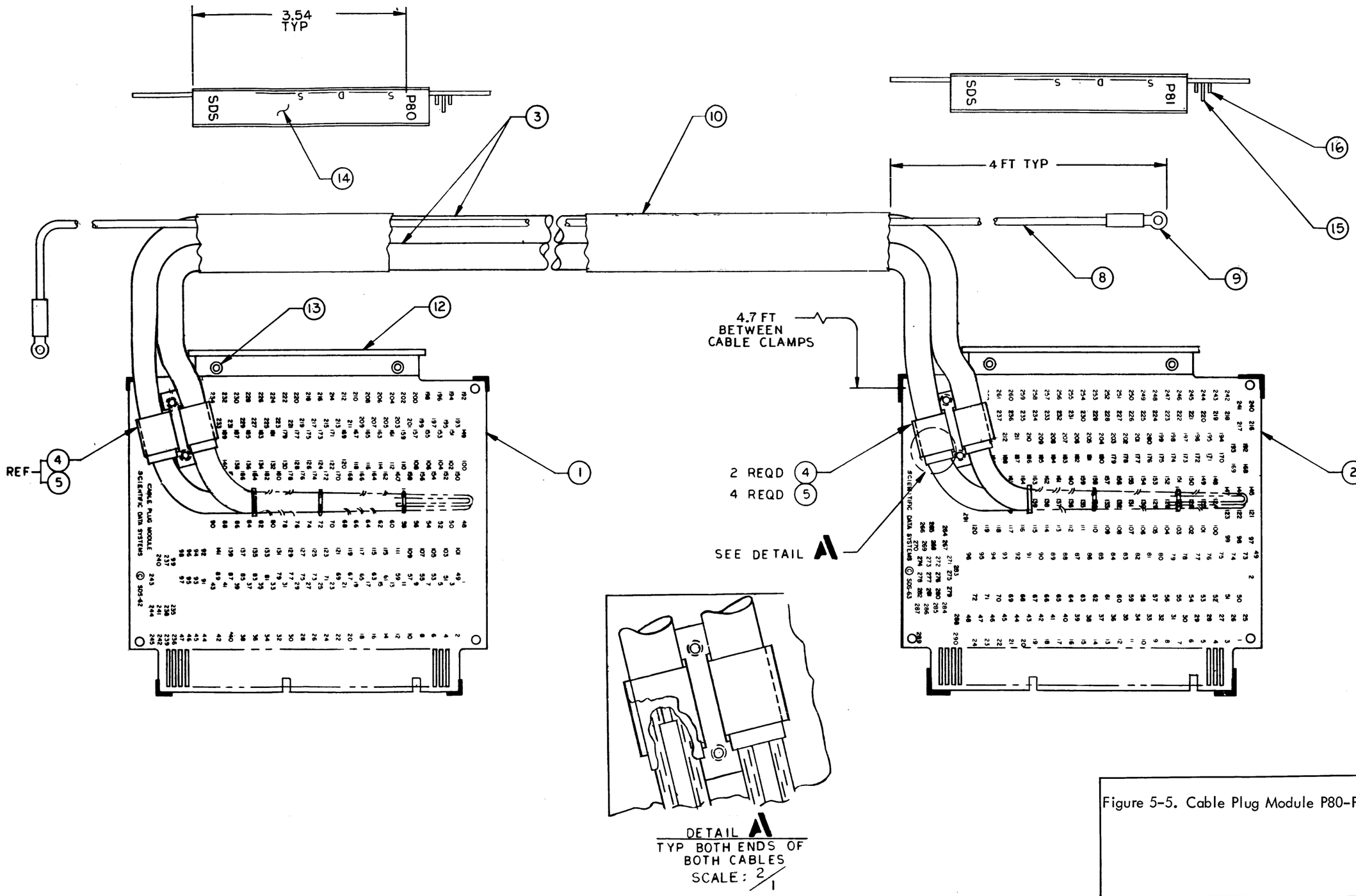
CHASSIS	LOCATION	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
01	TYPE	SX 58			1H 12	1H 12	1H 10	FH 15	FH 15			1H 10	1H 10	1H 10	GK 51	GH 10	GH 14	GH 14	FH 15	FH 15	FH 15
	KEY	4 24			10 34	10 34	2 44	8 30	8 30			2 44	2 44	2 44	2 22	2 40	30 34	30 34	8 30	8 30	8 30

CHASSIS	LOCATION	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
02	TYPE	1H 12	1H 12	1H 12	1H 11	1H 11	FH 15	FH 15	GH 11	1H 10	1H 10	GK 51	GK 51	GH 14	GH 14	GH 14	GH 10	GH 10	GH 10	FH 19	FH 15
	KEY	10 34	10 34	10 34	2 16	2 16	8 30	8 30	10 26	2 44	2 44	2 22	2 22	30 34	30 34	30 34	2 40	2 40	2 40	16 40	8 30

CHASSIS	LOCATION	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
03	TYPE		P 81	P 83	P 83	ZX 49		AX 14	AX 14	AX 14	AX 14	IK 51	1H 12	1H 12	1H 12	1H 12	1H 10	1H 10	GK 51		CX 13
	KEY		6 32	6 32	6 36	6 28		20 24	20 24	20 24	20 24	2 8	10 34	10 34	10 34	10 34	2 44	2 44	2 22		16 30

Figure 5-4. Model 9448 Assembly

107550-1B



DETAIL A
TYP BOTH ENDS OF BOTH CABLES
SCALE: 2/1

Figure 5-5. Cable Plug Module P80-P81 Assembly

107803-1E

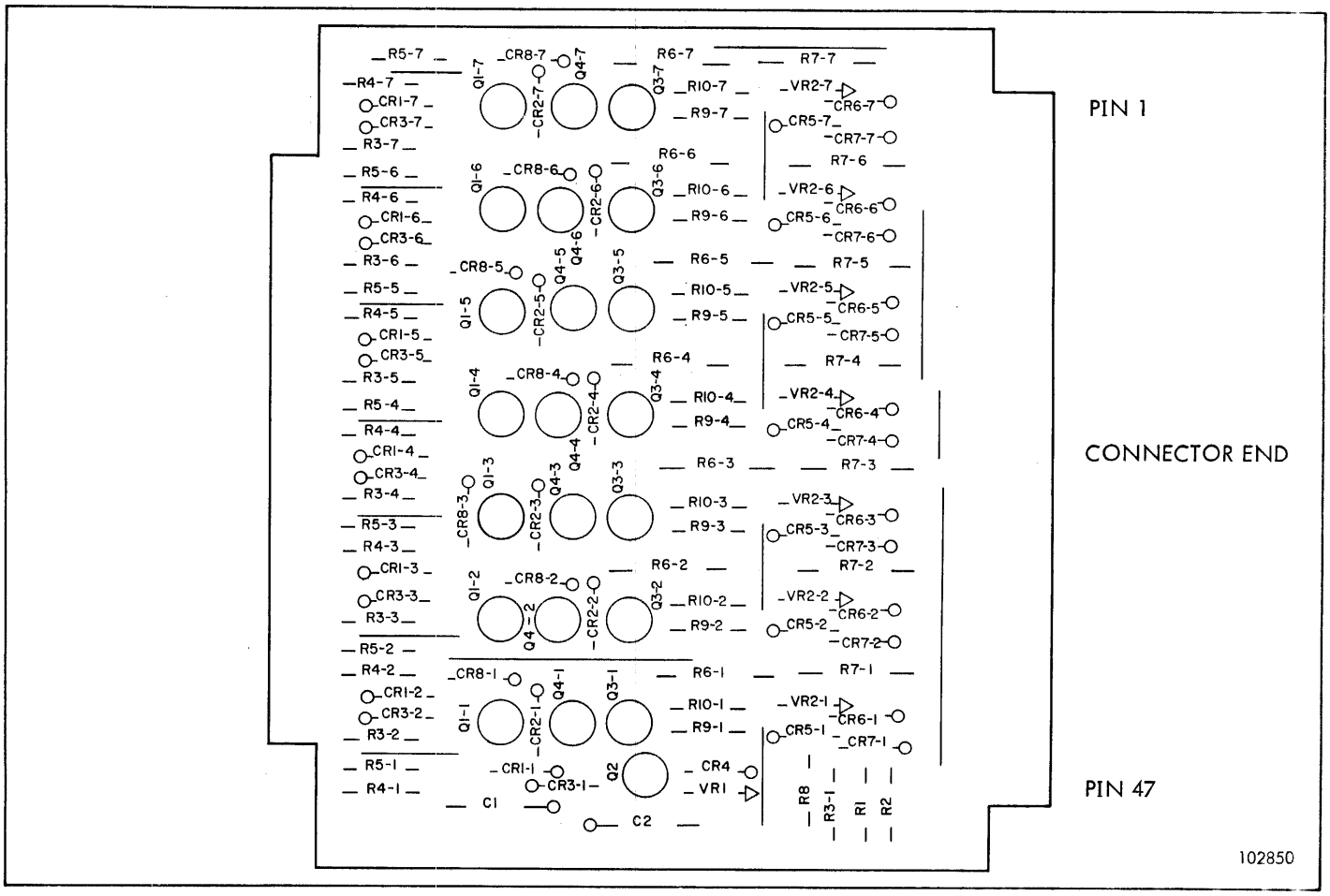


Figure 5-6. Cable Driver AX14 Parts Location

Table 5-3. Cable Driver AX14 Replaceble Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-6	Cable Driver AX14 (See tables 5-1 and 5-2 for next assembly)		SDS	102853	
	. Capacitor, tantalum, 4.7 μf, 20%, 50v	C1, C2	22, 23, 77		2
	. Diode	CR1, CR3 thru CR8	4, 12, 13, 14	1N914A	43
	. Diode	CR2	13, 15, 28	1N921	7
	. Diode	VR1, VR2	2, 12, 13, 14	1N746	8
	. Resistor, 3.9k, 2%, 1/2w	R1, R2, R4, R5	16, 17		16
	. Resistor, 8.2k, 2%, 1/2w	R3	16, 17		7
	. Resistor, 22k, 2%, 1/2w	R8, R10	16, 17		8
	. Resistor, 39k, 2%, 1/2w	R9	16, 17		7
	. Transistor, SDS 209	Q1, Q2, Q4	7 1 3	2N2477 2N2538 2N2848	15
	. Transistor, SDS 220	Q3	3, 11 1	2N2369 2N2501	7

Table 5-4. Crystal Clock Generator CX13 Replaceable Parts

Fig. & Index No.	Description	Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-7	Crystal Clock Generator CX13 (See table table 5-2 for next assembly)		SDS	102171	
	. Capacitor, tantalum, 15 µf, 20%, 20v	C1, C5	22, 23, 76		2
	. Capacitor, mica, 100 pf, 5%	C2	19, 20, 21		1
	. Capacitor, mica, 47 pf, 5%	C3, C4	19, 20, 21		2
	. Capacitor, mica, 150 pf, 5%	C6, C7	19, 20, 21		2
	. Capacitor, mica, 470 pf, 5%	C8	19, 20, 21		1
	. Capacitor, mylar, 1500 pf, 10%	C9	26, 27, 74		1
	. Capacitor, mylar, 4700 pf, 10%	C10	26, 27, 74		1
	. Capacitor, mica, 510 pf, 5%	C11	19, 20, 21		1
	. Capacitor, tantalum, 4.7 µf, 20%, 50v	C12	23, 77		1

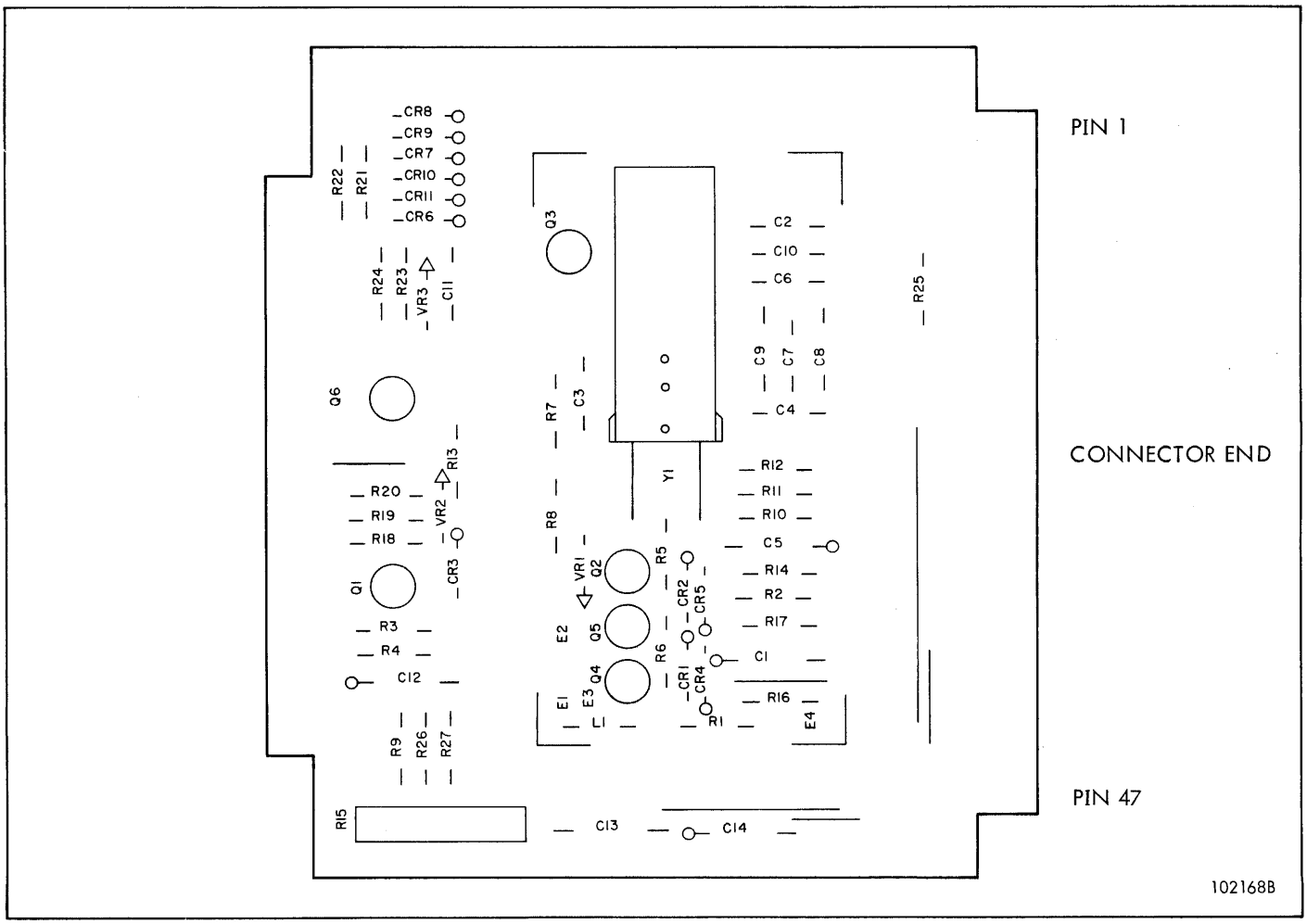


Figure 5-7. Crystal Clock Generator CX13 Parts Location

Table 5-4. Crystal Clock Generator CX13 Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-7 (Cont.)	. Crystal*	Y1	138		1
	. Diode	CR1-CR11	4, 12, 13, 14	1N914A	11
	. Diode	VR1	2, 12, 13, 14	1N752	1
	. Diode	VR2, VR3	2, 12, 13, 14	1N746	2
	. Potentiometer, 1k, 10%	R15	35, 44		1
	. Resistor, 1k, 2%, 1/2w	R1, R2, R5, R6, R9	16, 17		5
	. Resistor, 3.9k, 2%, 1/2w	R3, R16, R21, R22	16, 17		4
	. Resistor, 820 ohms, 2%, 1/2w	R4, R23	16, 17		2
	. Resistor, 2.2k, 2%, 1/2w	R7	16, 17		1
	. Resistor, 100 ohms, 2%, 1/2w	R8	16, 17		1
	. Resistor, 1.5k, 2%, 1/2w	R10	16, 17		1
	. Resistor, 4.7k, 2%, 1/2w	R11, R14	16, 17		2
	. Resistor, 15k, 2%, 1/2w	R12	16, 17		1
	. Resistor, 10k, 2%, 1/2w	R13	16, 17		1
	. Resistor, 18k, 2%, 1/2w	R17	16, 17		1
	. Resistor, 3.3k, 2%, 1/2w	R18, R19, R20	16, 17		3
	. Resistor, 39k, 2%, 1/2w	R24	16, 17		1
	. Resistor, 47 ohms, 2%, 1/2w	R25	16, 17		1
	. Transistor, SDS 220	Q1-Q5,	3, 11 1 95	2N2369 2N2501 2N2710	5
	. Transistor, SDS 209	Q6	1 7 3	2N2538 2N2476 2N2848	1

*Crystal shall be housed in Military Holder type HC-6/U, HC-13/U or HC-13/U with a 2.0-inch cover, and shall be adjusted to have the required frequency in series resonance at 60°C. The crystal cut and mode shall be determined as follows:

Frequency Range (Kc)	Cut	Mode
30 - 100	N	Flexure
100 - 250	E	Extension
250 - 500	C	Face shear
500 - 2000	A	Thickness shear

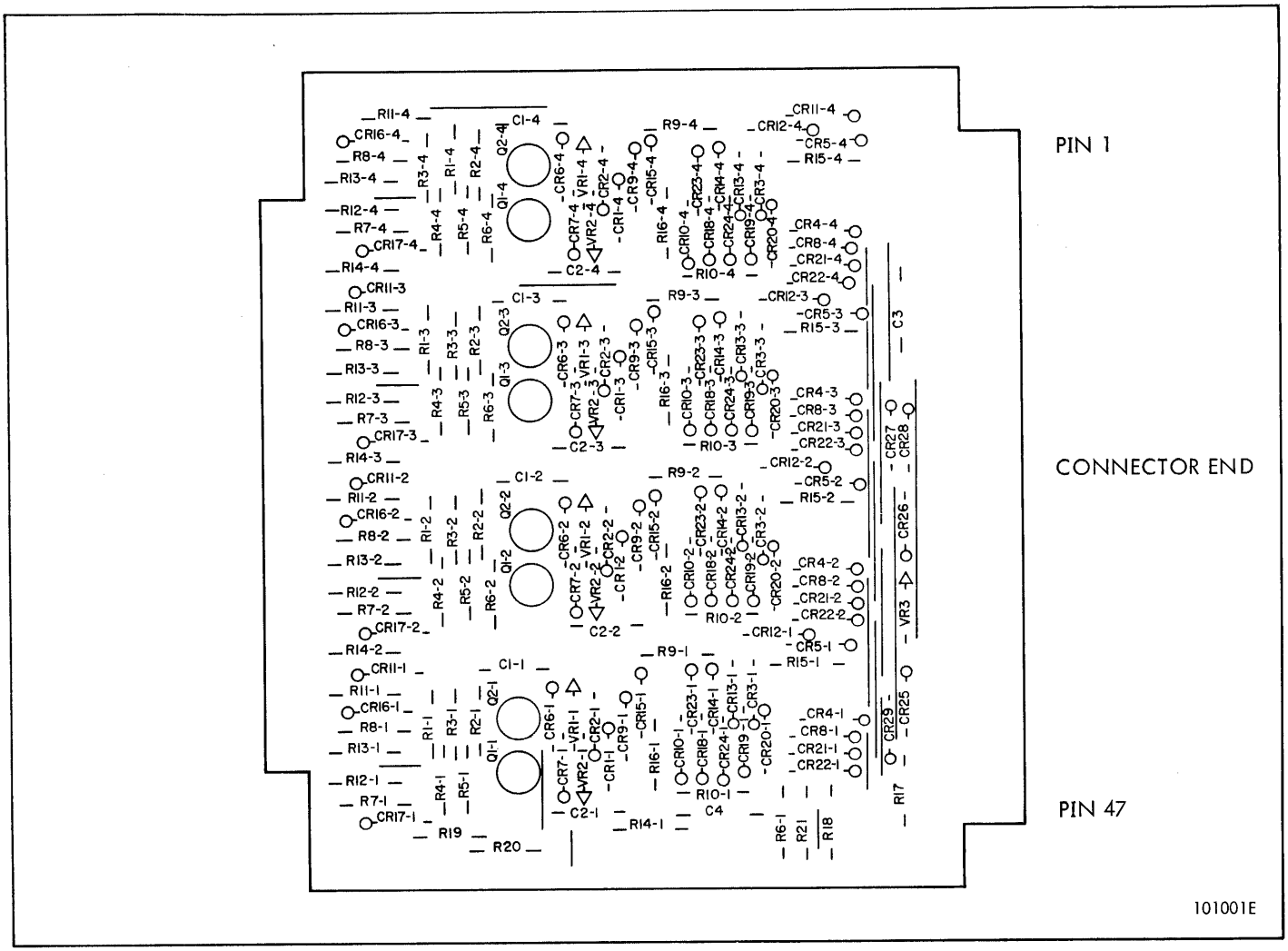


Figure 5-8. Counter Flip-Flop FH15 Parts Location

Table 5-5. Counter Flip-Flop FH15 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-8	Counter Flip-Flop FH15 (See table 5-2 for next assembly)		SDS	101026	
	. Capacitor, mica, 330 pf, 5%	C1, C2	19, 20, 21		8
	. Capacitor, mylar, 0.01 μf, 10%	C3, C4	26, 27, 74		2
	. Diode	CR1-CR29	4, 12, 13, 14	1N914A	101
	. Diode	VR1, VR2	2, 12, 13, 14	1N746	8
	. Diode	VR3	2, 12, 13, 14	1N752	1
	. Resistor, 3.9k, 2%, 1/2w	R1, R6, R17	16, 17		9
	. Resistor, 10k, 2%, 1/2w	R2, R5	16, 17		8
	. Resistor, 5.6k, 2%, 1/2w	R3, R4	16, 17		8

Table 5-5. Counter Flip-Flop FH15 Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-8 (Cont.)	. Resistor, 470 ohms, 2%, 1/2w	R7, R8, R21	16, 17		9
	. Resistor, 120 ohms, 2%, 1/2w	R9, R10, R15, R16	16, 17		16
	. Resistor, 470k, 2%, 1/2w	R11, R14	16, 17		8
	. Resistor, 100k, 2%, 1/2w	R12, R13	16, 17		8
	. Resistor, 4.7k, 2%, 1/2w	R18	16, 17		1
	. Resistor, 47k, 2%, 1/2w	R19, R20	16, 17		2
	. Transistor, SDS 200	Q1, Q2	1, 5, 7, 95	2N834	8

Table 5-6. DC Flip-Flop FH19 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-9	DC Flip-Flop FH19 (See tables 5-1 and 5-2 for next assembly)		SDS	103134	
	. Capacitor, mylar, 0.01 μf, 10%	C1	26, 27, 74		1
	. Diode	CR1-CR11	4, 12, 13, 14	1N914A	66
	. Diode	VR1, VR2	2, 12, 13, 14	1N746	12
	. Resistor, 3.9k, 2%, 1/2w	R1, R2, R5, R6	16, 17		24
	. Resistor, 820 ohms, 2%, 1/2w	R3, R4	16, 17		12
	. Resistor, 18k, 2%, 1/2w	R7, R8	16, 17		12
	. Resistor, 47k, 2%, 1/2w	R9	16, 17		1
	. Transistor, SDS 200	Q1, Q2	1, 5, 7, 95	2N834	12

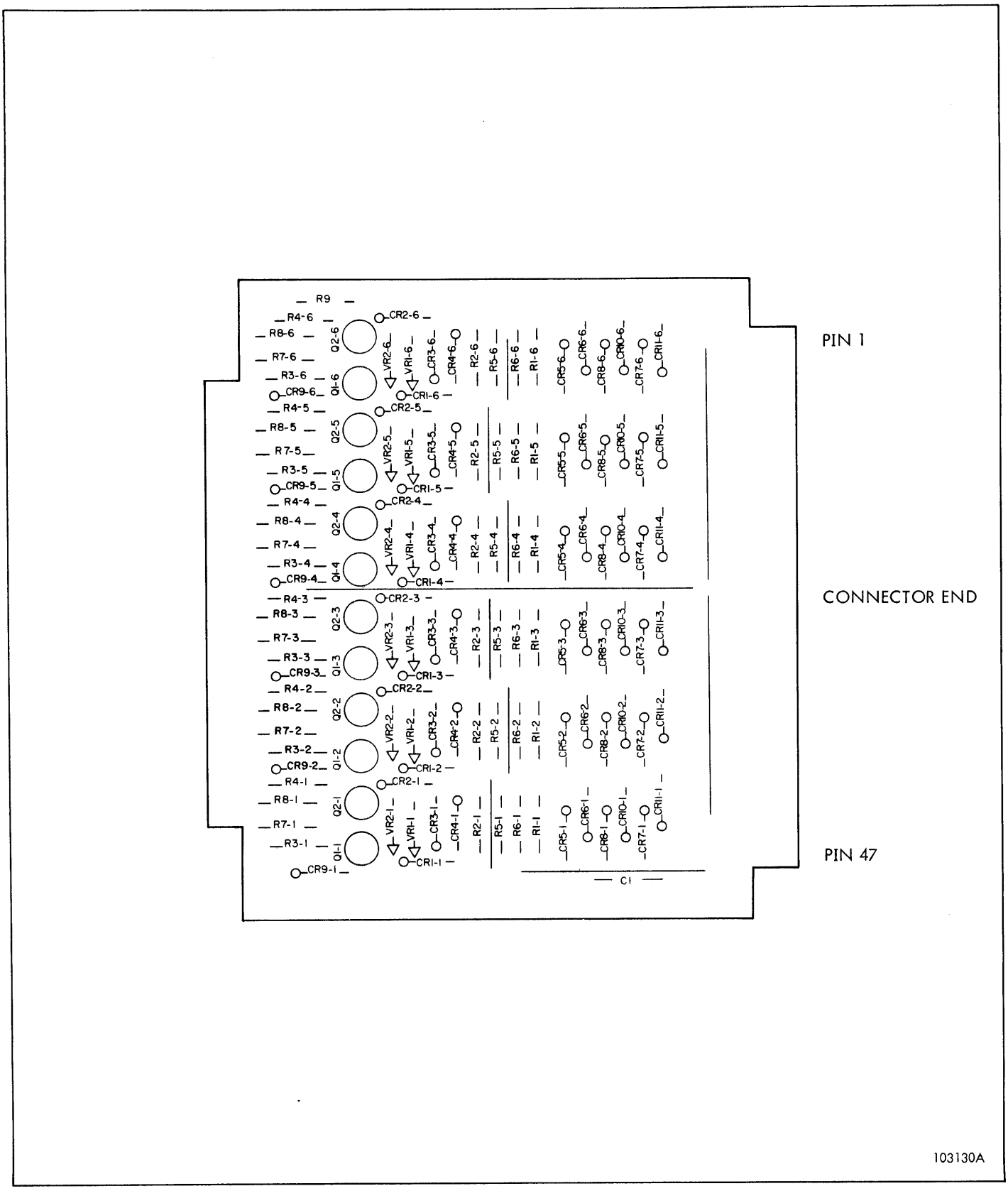


Figure 5-9. DC Flip-Flop FH19 Parts Location

Table 5-7. Gate Expander GH10 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-10	Gate Expander GH10 (See table 5-2 for next assembly)		SDS	100149	
	. Diode	CR1-CR31	4, 12, 13, 14	1N914A	31
	. Resistor, 3.9k, 2%, 1/2w	R1-R7	16, 17		7

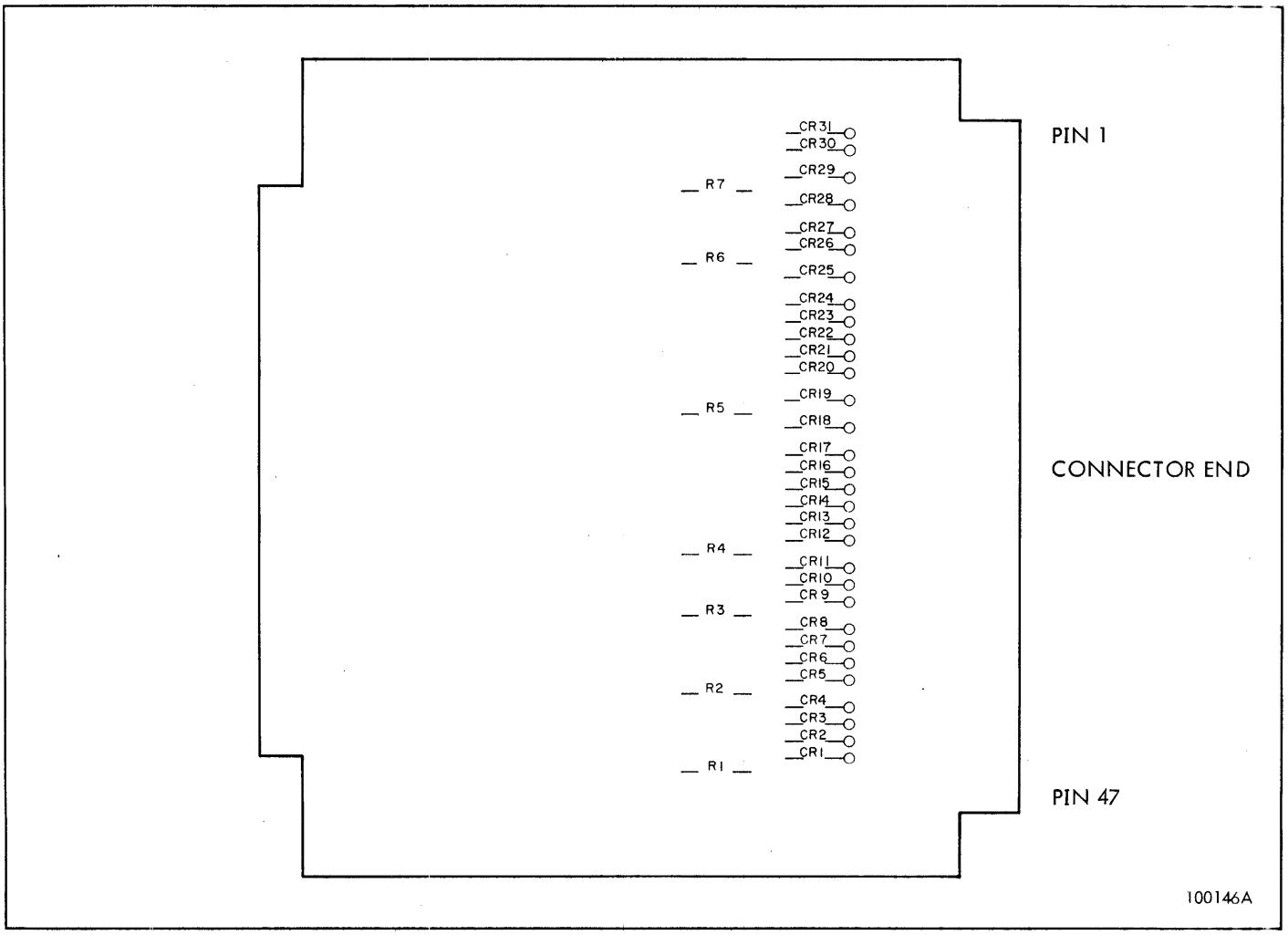


Figure 5-10. Gate Expander GH10 Parts Location

Table 5-8. Gate Expander GH11Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-11	Gate Expander GH11 (See table 5-2 for next assembly)		SDS	101769	
	. Diode	CR1-CR12	4, 12, 13, 14	1N914A	93
	. Resistor, 3.9k, 2%, 1/2w	R1-R4	16, 17		31

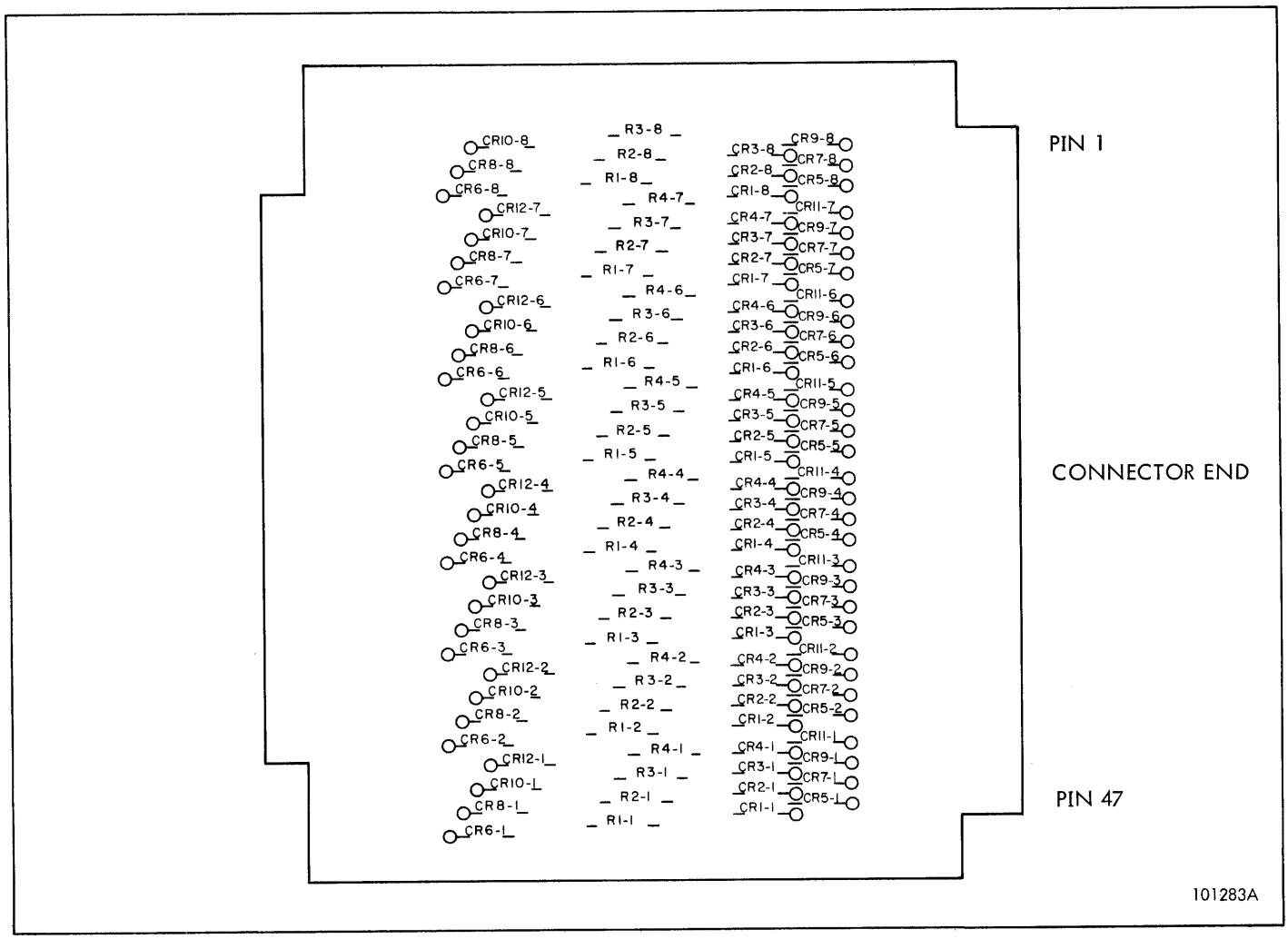


Figure 5-11. Gate Expander GH11 Parts Location

Table 5-9. Gate Expander GH14 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-12	Gate Expander GH14 (See table 5-2 for next assembly)		SDS	104431	
	. Diode	CR1-CR24	4, 12, 13, 14	1N914A	24
	. Resistor, 3.9k, 2%, 1/2w	R1-R7	16, 17		7

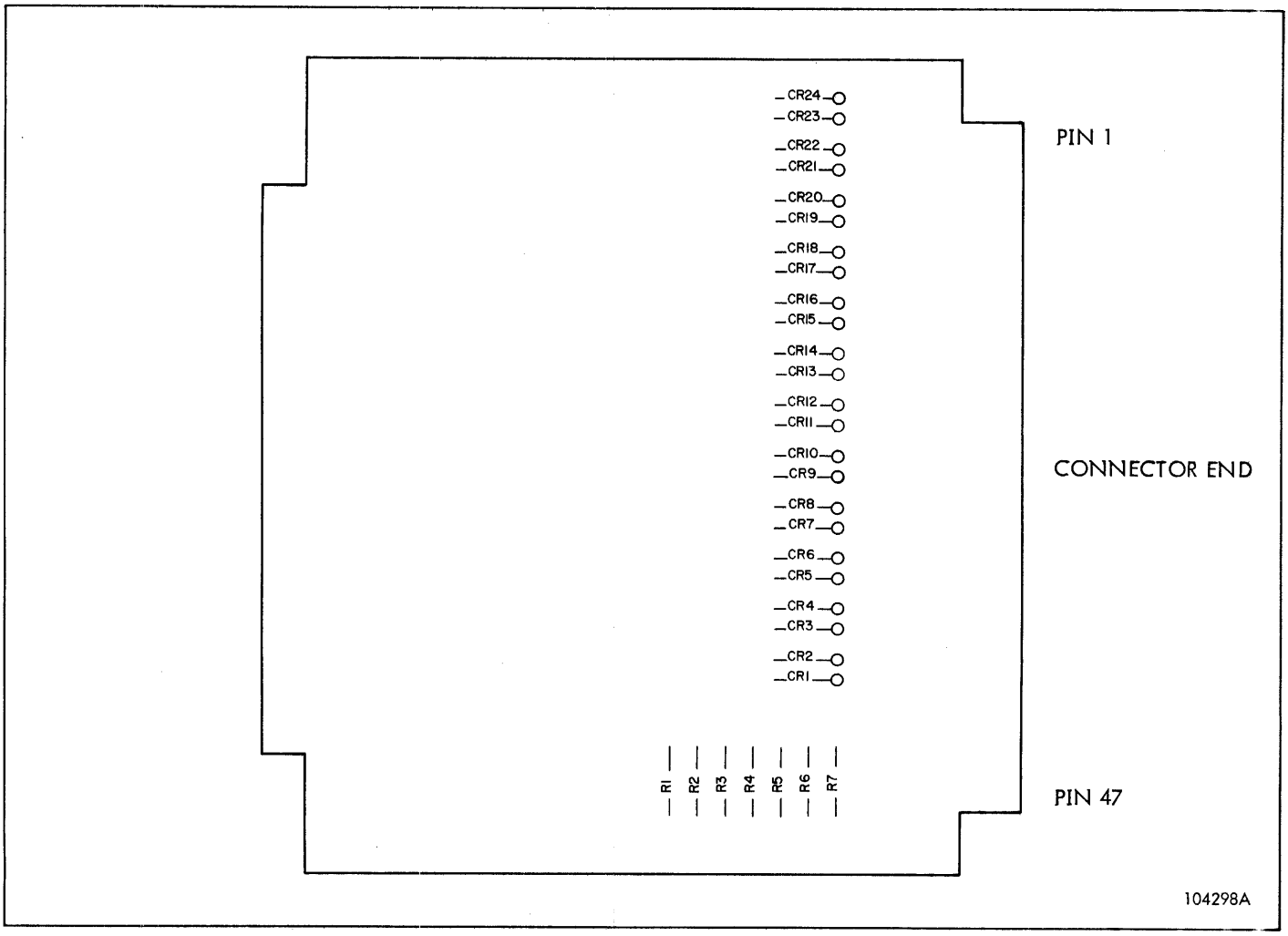


Figure 5-12. Gate Expander GH14 Parts Location

Table 5-10. Diode Gate No. 1 GK51 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-13	Diode Gate No. 1 GK51 (See tables 5-1 and 5-2 for next assembly)		SDS	100246	
	. Diode	CR1-CR36	4, 13 4, 12, 13, 14 4, 6 4	1N907A 1N914A 1N3063 1N3065	36
	. Resistor, 3.9k, 2%, 1/2w	R1-R9	16, 17		9

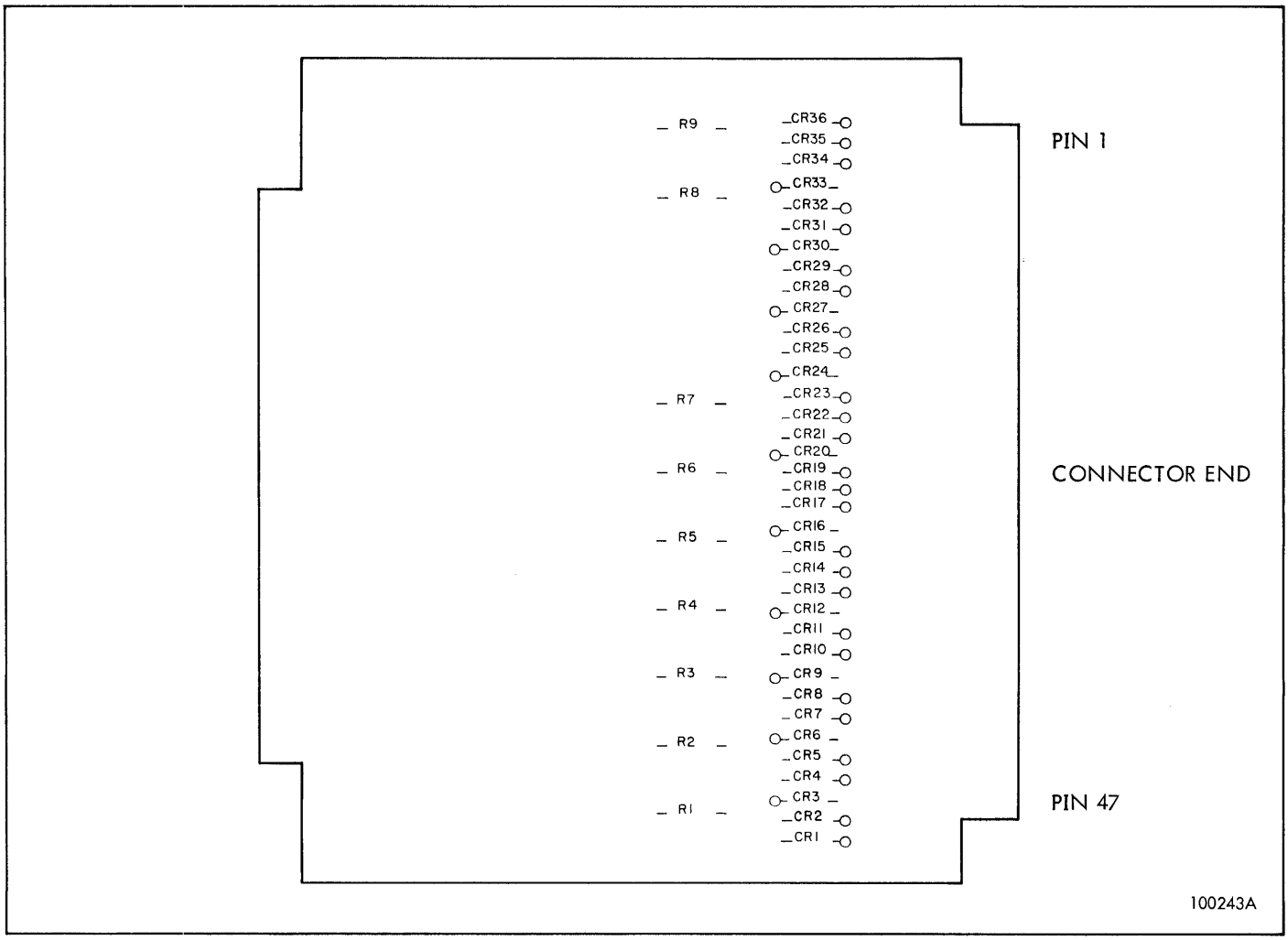


Figure 5-13. Diode Gate No. 1 GK51 Parts Location

Table 5-11. Data Amplifier HX29 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-14	Data Amplifier HX29 (See table 5-1 for next assembly)		SDS	103387	
	. Capacitor, mylar, 4700 pf, 10%	C1	23, 25, 191, 192, 193		1
	. Capacitor, mylar, 0.01 µf, 10%	C2	23, 25, 191, 192, 193		1
	. Capacitor, mylar, 2200 pf, 10%	C3, C5	23, 25, 191, 192, 193		2
	. Capacitor, tantalum, 4.7 µf, 20%, 50v	C4	11, 22, 23, 24, 192, 202		1
	. Capacitor, tantalum, 47 µf, 20%, 20v	C7, C11 thru C14	11, 22, 23, 24, 192, 202		5
	. Capacitor, mica, 39 pf, 5%	C8	19, 20, 188, 189		1
	. Capacitor, mylar, 0.015 µf, 10%	C10	23, 25, 191, 192, 193		1
	. Diode, SDS 103	CR1-CR5	3, 5, 10, 11, 14, 225	1N914A	5
	. Diode, SDS 101	VR1-VR3	1, 11, 14, 269	1N746	3
	. Diode, SDS 106	VR4-VR13	1, 10, 11, 14	1N752	10
	. Inductor, molded, 10 mh	L1	41, 70, 90, 91		1
	. Integrated circuit, SDS 302	A1	3		1
	. Potentiometer, 2k	R6, R31, R34	35, 36		3
	. Potentiometer, 20k	R10	35, 36		1
	. Resistor, 470 ohms, 2%, 1/2w	R1, R51, R53	11, 16, 17, 36, 176		3
	. Resistor, 68 ohms, 2%, 1/2w	R2	11, 16, 17, 36, 176		1
	. Resistor, 10k, 2%, 1/2w	R3, 5, 14, 16, 19, 33, 38, 39, 40, 41	11, 16, 17, 36, 176		13
	. Resistor, 1k, 2%, 1/2w	R4, 7, 8, 29, 37	11, 16, 17, 36, 176		5
	. Resistor, 270k, 2%, 1/2w	R9	11, 16, 17, 36, 176		1
	. Resistor, 100k, 2%, 1/2w	R11, 46	11, 16, 17, 36, 176		2
	. Resistor, 47 ohms, 2%, 1/2w	R12	11, 16, 17, 36, 176		1
	. Resistor, 3.3k, 2%, 1/2w	R13, 32	11, 16, 17, 36, 176		2
	. Resistor, 1.8k, 2%, 1/2w	R15, 28	11, 16, 17, 36, 176		2

Table 5-11. Data Amplifier HX29 Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-14 (Cont.)	. Resistor, 4.7k, 2%, 1/2w	R17, 18, 20, 27, 30, 42, 48, 49, 50	11, 16, 17, 36, 176		9
	. Resistor, 8.2k, 2%, 1/2w	R21-R24	11, 16, 17, 36 176		4
	. Resistor, 39k, 2%, 1/2w	R25	11, 16, 17, 36, 176		1
	. Resistor, 22k, 2%, 1/2w	R26	11, 16, 17, 36, 176		1
	. Resistor, 10k, 2%, 1/2w	R35, 36, 43	11, 16, 17, 36, 176		3
	. Resistor, 220 ohms, 2%, 1/2w	R44, 52, 54	11,16, 17, 36, 176		3
	. Resistor, 27k, 2%, 1/2w	R45	11, 16, 17, 36, 176		1
	. Resistor, 6.8k, 2%, 1/2w	R47	11, 16, 17, 36, 176		1
	. Transistor, SDS 205	Q1, 2, 5, 6, 7, 8, 12, 13 14	1, 3, 96	2N930	0
	. Transistor, SDS 214	Q4, 11	1, 3	2N2801	2
	. Transistor, SDS 203	Q9, 10, 15	1, 3, 11	2N2219	3

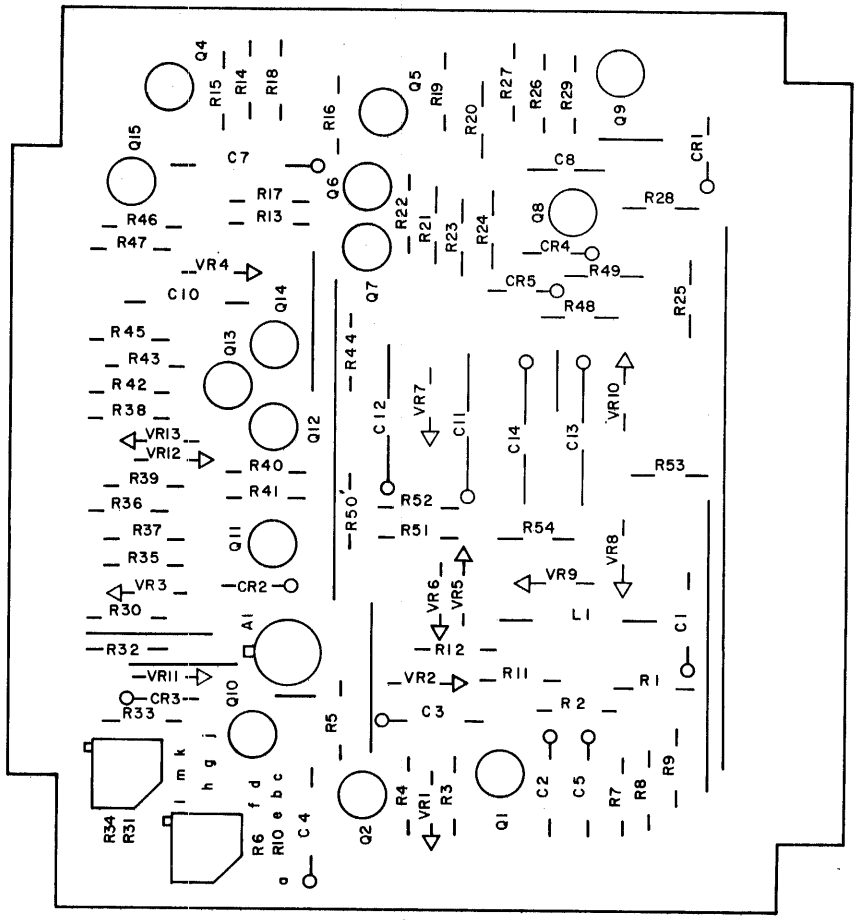


Figure 5-14. Data Amplifier HX29 Parts Location

Table 5-12. Read Amplifier HX30 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-15	Read Amplifier HX30 (See table 5-1 for next assembly)		SDS	107370	
	. Capacitor, tantalum, 47 μf, 20%, 20v	C1, C2	11, 22, 23, 24, 192, 202		2
	. Diode, SDS 104	CR1	3, 5, 14, 63	1N3600	4
	. Diode, SDS 103	CR2, CR3	3, 5, 10, 11, 14, 225	1N914A	8
	. Diode, SDS 106	VR1-VR8	1, 10, 11, 14	1N752	14
	. Resistor, 5.6k, 2%, 1/2w	R1	11, 16, 17, 36, 176		4
	. Resistor, 39k, 2%, 1/2w	R2-R4	11, 16, 17, 36, 176		12
	. Resistor, 82k, 2%, 1/2w	R5, R8	11, 16, 17, 36, 176		8
	. Resistor, 100 ohms, 2%, 1/2w	R6, R7	11, 16, 17, 36, 176		8
	. Resistor, 15k, 2%, 1/2w	R9, R10	11, 16, 17, 36, 176		8
	. Resistor, 1.2k, 2%, 1/2w	R11	11, 16, 17, 36, 176		1
	. Resistor, 910 ohms, 2%, 1/2w	R12	11, 16, 17, 36, 176		1
	. Resistor, 75k, 2%, 1/2w	R13	11,16, 17 36, 176		1
	. Resistor, 6.8k, 2%, 1/2w	R14	11, 16, 17 36, 176		1
	. Resistor, 470 ohms, 2%, 1/2w	R15	11, 16, 17 36, 176		1
	. Transistor, SDS 201	Q1	1, 3, 5	2N2369	4
	. Transistor, SDS 205	Q2-Q5	1, 3, 96	2N930	13

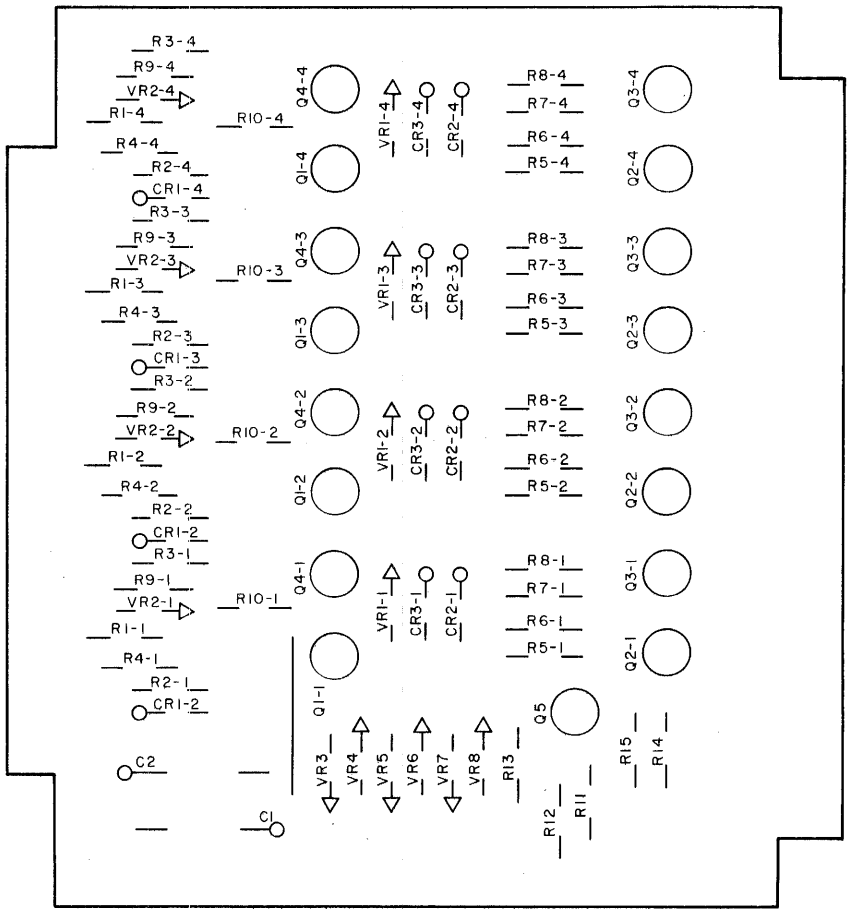


Figure 5-15. Read Amplifier HX30 Parts Location

Table 5-13. Gate Write Amplifier HX31 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-16	Gate Write Amplifier HX31 (See table 5-1 for next assembly)		SDS	107429	
	. Diode, SDS 103	CR1-CR11	3, 5, 10, 11, 14, 225	1N914A	44
	. Diode, SDS 101	VR1, VR2	1, 11, 14, 269	1N746	8
	. Resistor, 5.6k, 2%, 1/2w	R1, R2	11, 16, 17, 36, 176		8
	. Resistor, 39k, 2%, 1/2w	R3, R4	11, 16, 17, 36, 176		8
	. Resistor, 1.2k, 2%, 1/2w	R5, R6	11, 16, 17, 36, 176		8
	. Transistor, SDS 203	Q1, Q2	1, 3, 11	2N2219	8

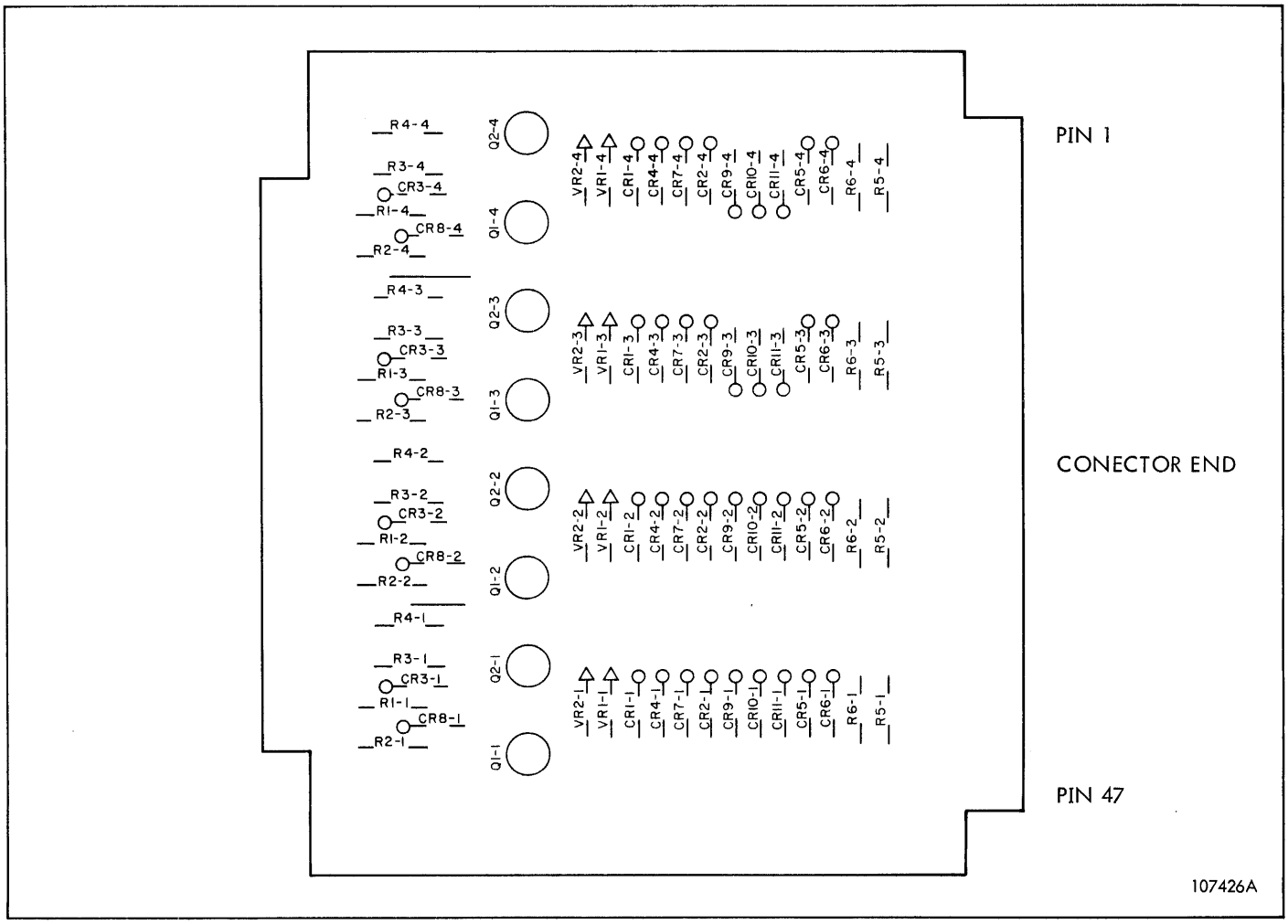


Figure 5-16. Gate Write Amplifier HX31 Parts Location

Table 5-14. Photo Sense Amplifier HX48 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-17	Photo Sense Amplifier HX48 (See table 5-1 for next assembly)		SDS	117696	
	. Capacitor, tantalum, 2.2 μf, 20%, 50v	C1	11, 22, 23, 24, 192, 202		4
	. Capacitor, tantalum, 1 μf, 20%, 50V	C2, C3	11, 22, 23, 24, 192, 202		2
	. Diode, SDS 107	CR1, CR6	3, 28, 225	1N921	8
	. Diode, SDS 103	CR2, CR5	3, 5, 10, 11, 14, 225	1N914A	8
	. Diode, SDS 101	VR1, VR2	1, 11, 14, 269	1N746	8
	. Diode, SDS 106	VR3-VR5	1, 10, 11, 14	1N752	3
	. Potentiometer, 50k	R1	35, 44, 45		4
	. Potentiometer, 100 ohms	R16	35, 44, 45		1
	. Resistor, 1.2k, 2%, 1/2w	R2	11, 16, 17, 36, 176		4
	. Resistor, 33k, 2%, 1/2w	R3	11, 16, 17, 36, 176		4
	. Resistor, 10k, 2%, 1/2w	R4	11, 16, 17, 36, 176		4
	. Resistor, 560 ohms, 2%, 1/2w	R5	11, 16, 17, 36, 176		4
	. Resistor, 68k, 2%, 1/2w	R6, R7	11, 16, 17, 36, 176		8
	. Resistor, 2.2k, 2%, 1/2w	R8, R11	11, 16, 17, 36, 176		8
	. Resistor, 12k, 2%, 1/2w	R9, R10	11, 16, 17, 36, 176		8
	. Resistor, 1.5k, 2%, 1/2w	R12, R13	11, 16, 17, 36, 176		2
	. Resistor, metal film, 1k, 2%, 1/2w	R14	11, 23, 36, 45, 73, 176, 185, 234		1
	. Resistor, 270 ohms, 2%, 1/2w	R15	11, 16, 17, 36, 176		1
	. Resistor, 220 ohms, 2%, 1/2w	R17	11, 16, 17, 36, 176		1
	. Resistor, 120 ohms, 2%, 1/2w	R18	11, 16, 17, 36, 176		1
	. Resistor, metal film, 18 ohms 2%, 1/2w	R19-R22	11, 23, 36, 45, 73, 176, 185, 234		4

Table 5-14. Photo Sense Amplifier HX48 Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-17 (Cont.)	. Transistor, SDS 205	Q1	1, 3, 96	2N930	4
	. Transistor, SDS 202	Q2, Q3	1, 3, 5, 7	2N914	8
	. Transistor, SDS 214	Q4	1, 3	2N2801	1
	. Transistor, SDS 210	Q5, Q6	3, 8, 141	2N2890	2

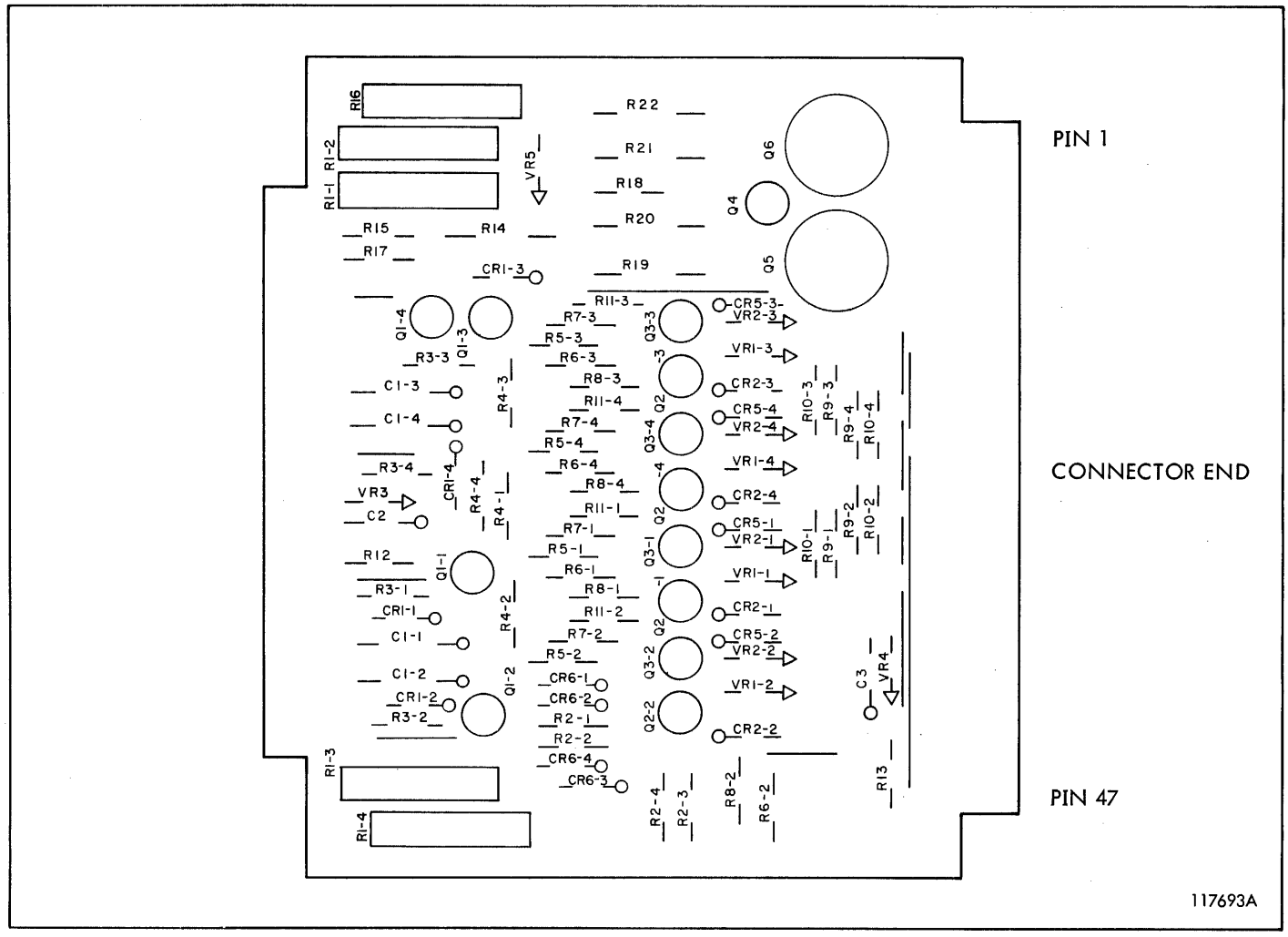


Figure 5-17. Photo Sense Amplifier HX48 Parts Location

Table 5-15. AND/OR Inverter IH10 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-18	AND/OR Inverter IH10 (See tables 5-1 and 5-2 for next assembly)		SDS	100137	
	. Capacitor, tantalum, 4.7 μf, 20%,50v	C1	23, 77		1
	. Diode	CR1-CR23	4, 12, 13, 14	1N914	23
	. Diode	VR1	2, 12, 13, 14	1N746	4
	. Resistor, 820 ohms, 2%, 1/2w	R1	16, 17		4
	. Resistor, 3.9k, 2%, 1/2w	R3-R10	16, 17		8
	. Resistor, 18k, 2%, 1/2w	R2	16, 17		4
	. Transistor, SDS 201	Q1	1 3, 11	2N2501 2N2369	4

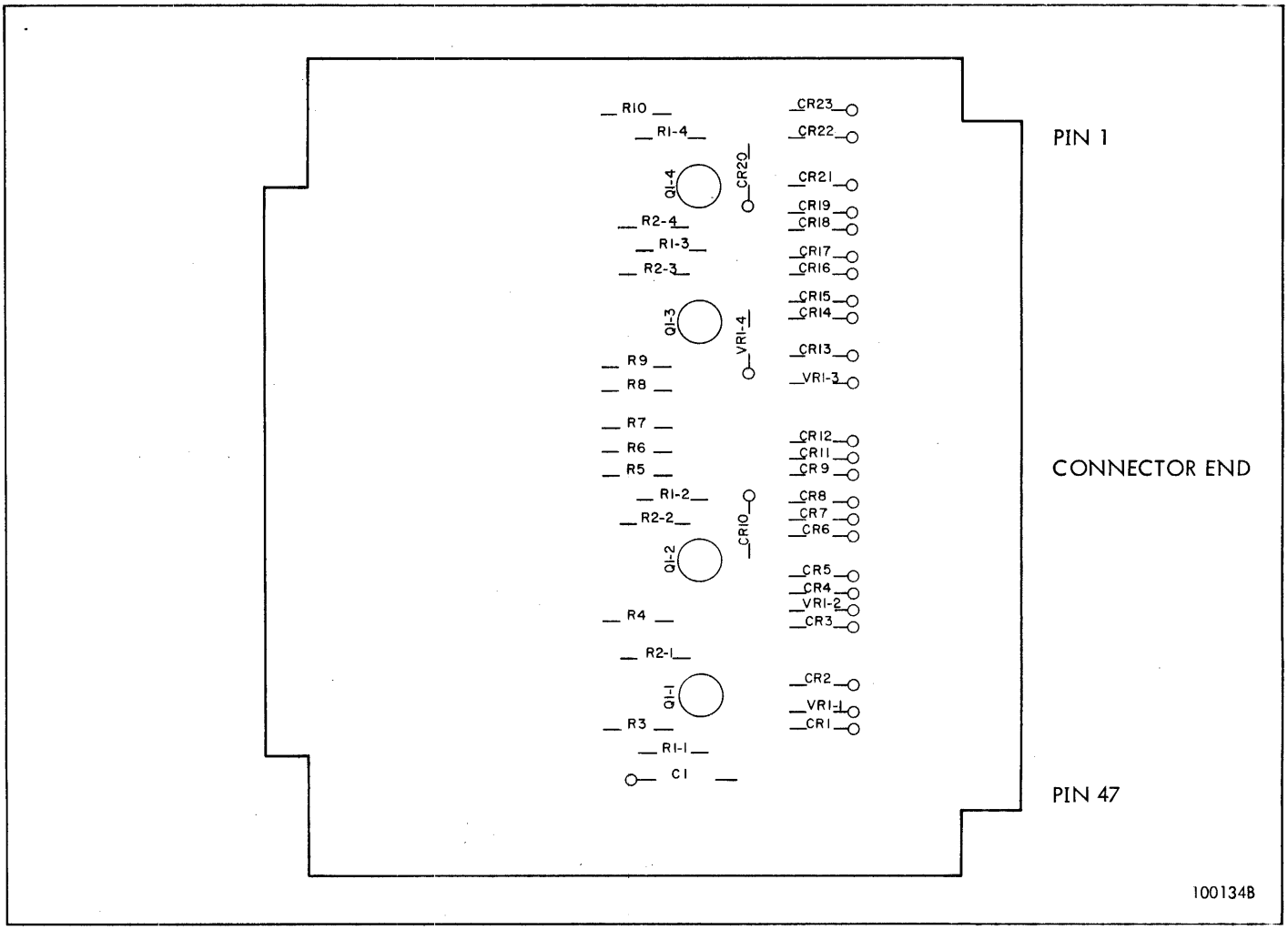


Figure 5-18. AND/OR Inverter IH10 Parts Location

Table 5-16. OR Gate Inverter IH11 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-19	OR Gate Inverter IH11 (See table 5-2 for next assembly)		SDS	100319	
	. Capacitor, tantalum, 4.7 μf, 20%, 50v	C1	23, 77		1
	. Diode	CR1-CR52	4, 12, 13, 14	1N914A	52
	. Diode	VR1	2, 12, 13, 14	1N746	4
	. Resistor, 820 ohms, 2%, 1/2w	R1	16, 17		4
	. Resistor, 18k, 2%, 1/2w	R2	16, 17		4
	. Resistor, 3.9k, 2%, 1/2w	R3-R28	16, 17		26
	. Transistor, SDS 200	Q1	1, 5, 7, 95	2N834	4

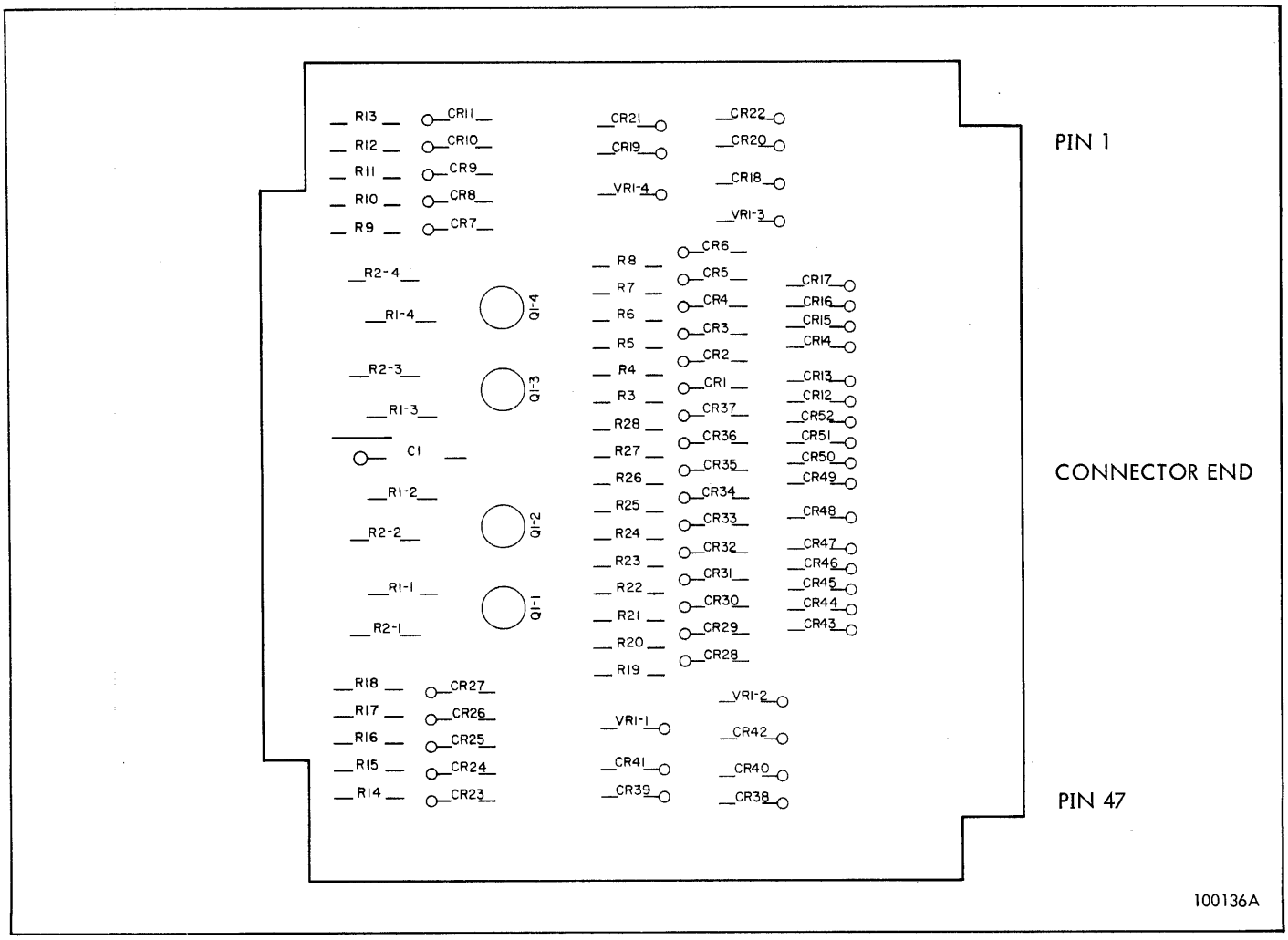


Figure 5-19. OR Gate Inverter IH11 Parts Location

Table 5-17. AND Inverter IH12 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-20	AND Inverter IH12 (See table 5-2 for next assembly)		SDS	101767	
	. Capacitor, tantalum, 4.7 μf, 20%, 50v	C1	23, 77		1
	. Diode	CR1-CR29	4, 12, 13, 14	1N914A	41
	. Diode	VR1-VR10	2, 12, 13, 14	1N746	14
	. Resistor, 3.9k, 2%, 1/2w	R1, 3, 5, 7, 13, 14, 17, 19, 21, 23, 26	16, 17		15
	. Resistor, 820 ohms, 2%, 1/2w	R2, 4, 6, 8, 15 18, 20, 22, 24, 25	16, 17		14
	. Resistor, 18k, 2%, 1/2w	R9-R12, R16, R27-R30, R41	16, 17		14
	. Transistor, SDS 209	Q1-Q10	1 3 7	2N2538 2N2848 2N2476	14

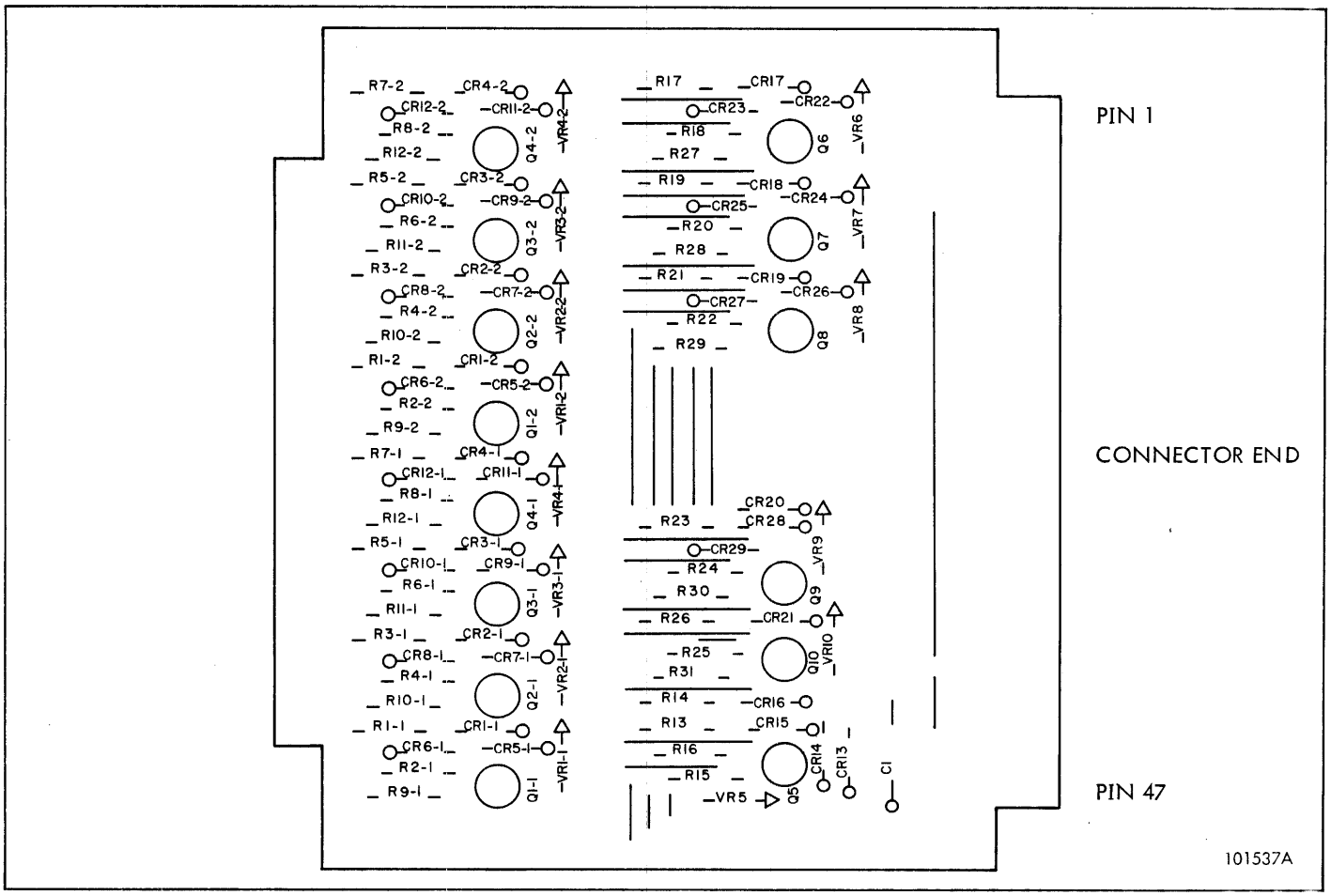


Figure 5-20. AND Inverter IH12 Parts Location

Table 5-18. Inverter Amplifier IK51 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-21	Inverter Amplifier IK51 (See tables 5-1 and 5-2 for next assembly)		SDS	100388	
	. Capacitor, silver mica, 68 pf, 5%	C1-C4	19, 20, 21		9
	. Capacitor, tantalum, 4.7 μf, 20%, 50v	C5	23, 77		1
	. Diode	CR1-CR10	4, 12, 13, 14	1N914A	16
	. Diode	VR1-VR6	2, 12, 13, 14	1N746	15
	. Resistive Termination Assy, 3 ea	AT1-AT4	72	56-590-65/3B	11
	. Resistor, 820 ohms, 2%, 1/2w	R1, 3, 6, 9, 12	16, 17		13
	. Resistor, 18k, 2%, 1/2w	R2, 4, 7, 10, 15	16, 17		13
	. Resistor, 3.9k, 2%, 1/2w	R5, 8, 26	16, 17		6
	. Resistor, 560 ohms, 2%, 1/2w	R11, 13, 16, 17, 19, 20, 21	16, 17		16
	. Resistor, 10k, 2%, 1/2w	R14	16, 17		3
	. Resistor, 470 ohms, 2%, 1/2w	R18	16, 17		2
	. Resistor, 15k, 2%, 1/2w	R22	16, 17		2
	. Resistor, 27k, 2%, 1/2w	R23-R25	16, 17		6
	. Transistor, SDS 201	Q1-Q8	1 3, 11 95	2N2501 2N2369 2N2710	20

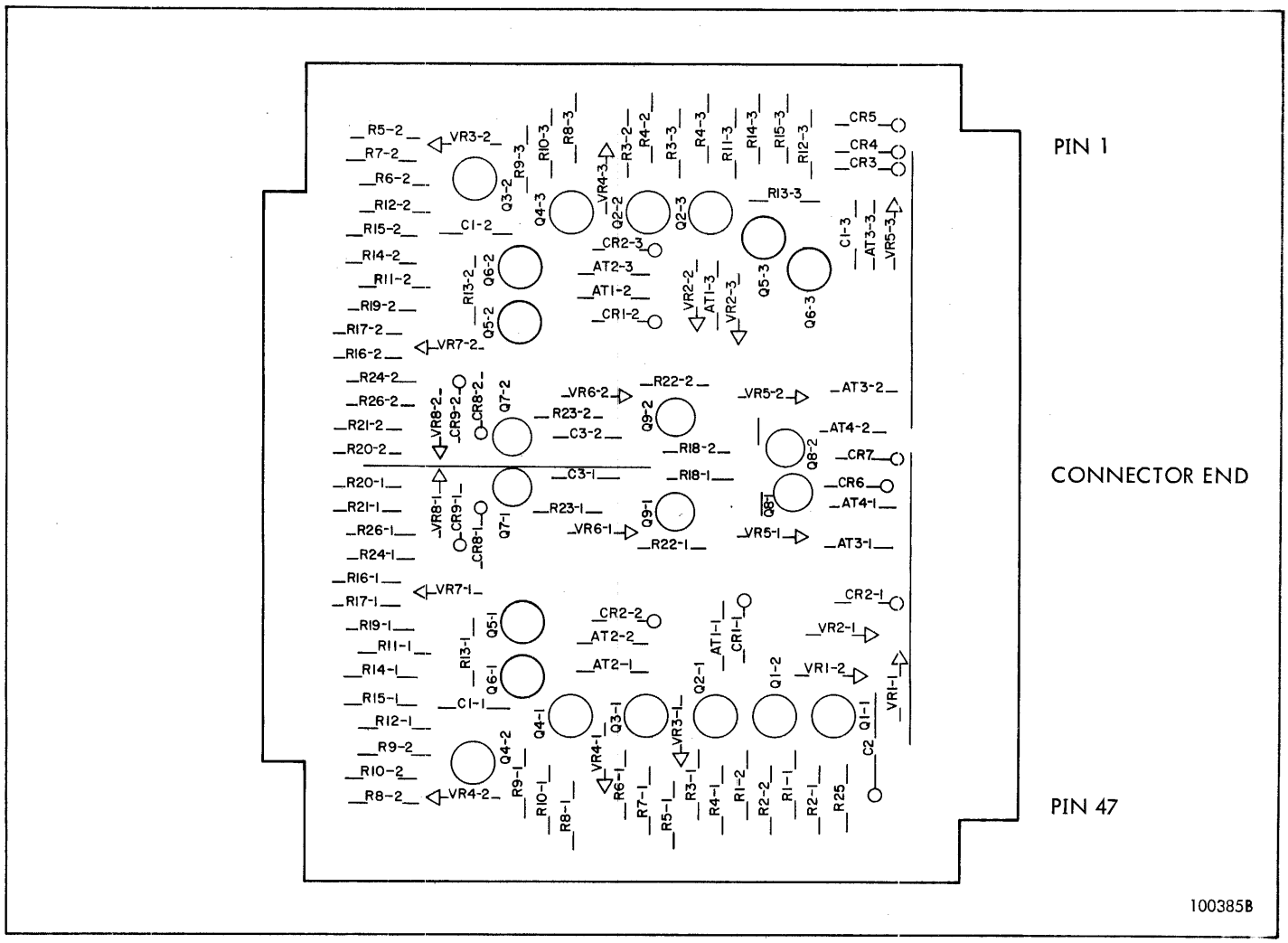


Figure 5-21. Inverter Amplifier IK51 Parts Location

Table 5-19. Relay Driver RK53 Replacement Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-22	Relay Driver RK53 (See table 5-1 for next assembly)		SDS	100905	
	. Capacitor, mylar, 3300 pf, 5%	C1, C4	26, 27, 74		8
	. Capacitor, mylar, 4700 pf, 5%	C2, C3	26, 27, 74		8
	. Capacitor, tantalum, 4.7 μf, 5%	C5	22, 23, 77		8
	. Diode	CR1, CR4 thru CR9	4, 13 4, 12, 13, 14 4, 6 4	1N907A 1N914A 1N3063 1N3065	28
	. Diode	CR2, CR3	13, 15, 28	1N921	8

Table 5-19. Relay Driver RK53 Replacement Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-22 (Cont.)	. Diode, Zener	VR1	2, 13, 14, 32	1N746	4
	. Resistor, 47k, 2%, 1/2w	R1, R7	16, 17		8
	. Resistor, 3.9k, 2%, 1/2w	R2	16, 17		4
	. Resistor, metal film, 100 ohms, 1%, 1w	R3	36, 38, 73		4
	. Resistor, metal film, 68 ohms, 1%, 1w	R4	36, 38, 73		4
	. Resistor, 22k, 2%, 1/2w	R5, R6	16, 17		8
	. Resistor, 4.7k, 2%, 1/2w	R8	16, 17		4
	. Transistor, SDS 203	Q1-Q3	1 29	2N2219 2N2404	12

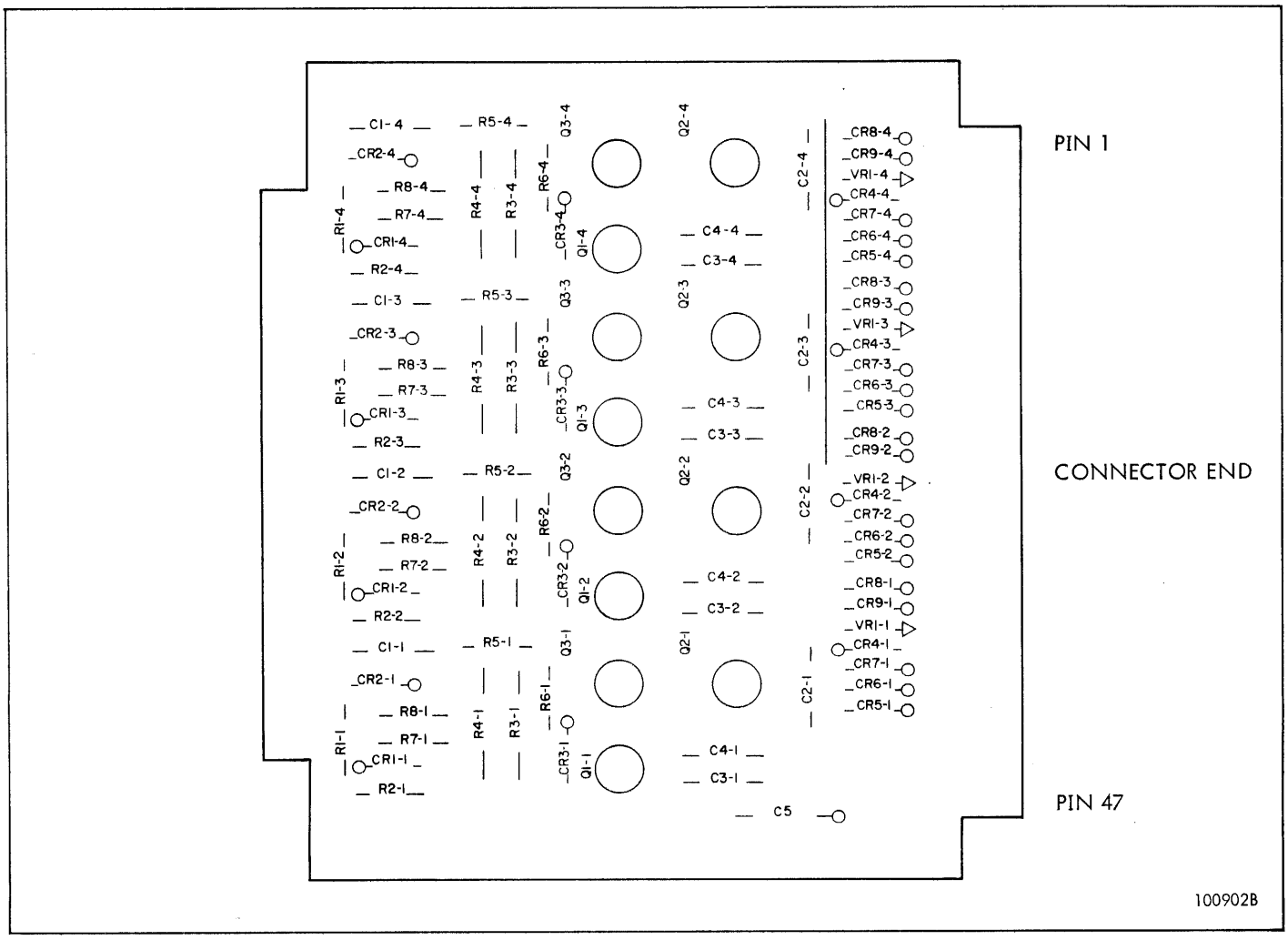


Figure 5-22. Relay Driver RK53 Parts Location

Table 5-20. Digital-to-Staircase Converter SK58 Replacement Parts

Fig. & Index No.	Description	Reference Designator	Supplier Code (See table 5-21)	Part No.	Qty
5-23	Digital-to-Staircase Converter SX58 (See table 5-2 for next assembly)		SDS	109413	
	. Capacitor, tantalum, 4.7 μf, 20%, 50v	C1, C2	11, 22, 23, 24, 192, 202		2
	. Diode, SDS 103	CR1-CR24	3, 5, 10, 11, 14, 225	1N914A	24
	. Resistor, 180 ohms, 2%, 1/2w	R1	11, 16, 17, 36, 176		1
	. Resistor, 18k, 2%, 1/2w	R2-R4	11, 16, 17, 36, 176		3
	. Resistor, 8.2k, 2%, 1/2w	R5-R13	11, 16, 17, 36, 176		9
	. Resistor, 560 ohms, 2%, 1/2w	R14-R16	11, 16, 17, 36, 176		3
	. Resistor, 33k, 2%, 1/2w	R17-R19	11, 16, 17, 36, 176		3

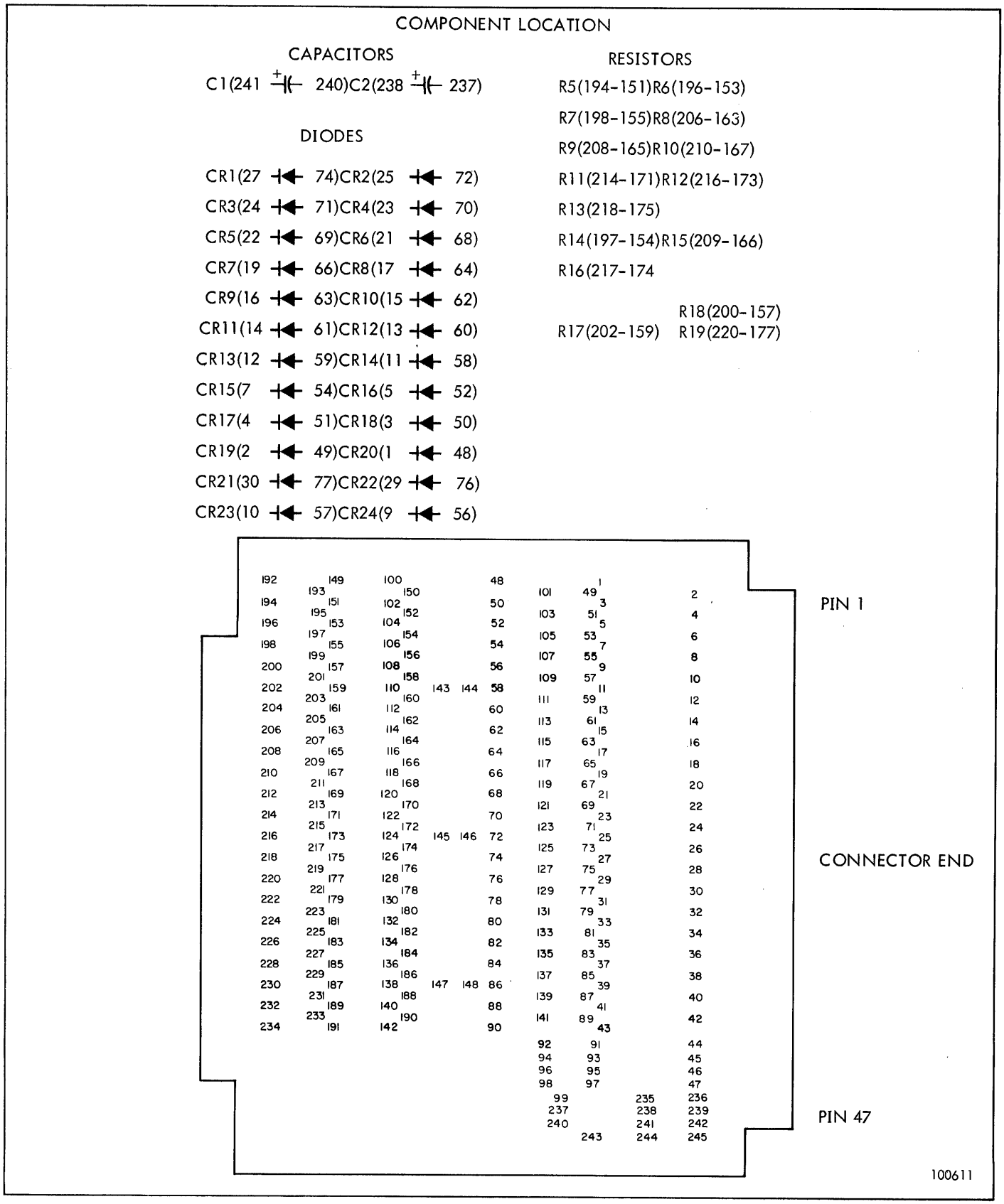


Figure 5-23. Digital-to-Staircase Converter SX58 Parts Location

Table 5-21. Supplier Code Index

Code No.	Name	Address
1	Motorola Semiconductor	5005 E. McDowell Rd. Phoenix, Arizona
2	Same as 1	
3	Fairchild Semiconductor	545 Whisman Road Mountain View, Calif.
4	Same as 3	
5	General Electric Co. Semiconductor Products Div.	Electronics Park Syracuse 1, N. Y.
6	Same as 5	
7	RCA Semiconductor Div.	Somerville, N. Y.
8	Silicon Transistor Corp.	East Gate Blvd. Garden City, N. Y.
10	Hughes Semiconductor Div.	500 Superior Ave. Newport Beach, Calif.
11	Texas Instruments, Inc.	P. O. Box 5012 Dallas, Texas
12	Same as 11	
13	Pacific Semiconductors, Inc.	1420 Aviation Blvd. Lawndale, Calif.
14	Continental Device Corp.	12515 Chadron Ave. Hawthorn, Calif.
15	Sperry Semiconductor Div.	380 Main Ave. Norwalk, Conn.
16	Corning Glass Works	550 High St. Bradford, Penn.
17	Welwyn International, Inc.	3535 Edgecliff Terr. Cleveland 11, Ohio
19	Arco Electronics, Inc.	Community Drive Great Neck, N. Y.
20	Sangamo Electric Co.	1207 N. 11th St. Springfield, Ill.
21	Micamold Electric Mfg. Co.	65 Gouverneur St. Newark, N. J.
22	Kemet Company	11901 Madison Ave. Cleveland 1, Ohio
23	Sprague Electric Co.	481 Marshall St. North Adams, Mass.
24	U. S. Semiconductor Products	3540 W. Osborn R. Phoenix, Ariz.
25	General Electric Co. Capacitor Dept.	Hudson Falls, N. Y.
26	Same as 23	
27	Same as 23	
28	Raytheon Semiconductor Co.	350 Ellis St. Mountain View, Calif.
30	General Instrument Corp.	65 Gouverneur St. Newark, N. J.
35	Bourns, Inc.	1200 Columbia Ave. Riverside, Calif.
36	International Resistance Co.	401 N. Broad St. Philadelphia, Penn.
38	Same as 23	
41	Delevan Electronics Corp.	77 Olean Road East Aurora, N. Y.
42	Same as 41	
44	Atohm Electronics	7648 San Fernando Road Sun Valley, Calif.
45	Dale Electronics, Inc.	P. O. Box 609 Columbus, Nebraska
48	Littelfuse, Inc.	1865 Miner St. Des Plaines, Illinois
49	Bussman Mfg. Co.	University at Jefferson St. Louis, Missouri
51	Cinch Jones Division	1026 S. Homan Ave. Chicago, Ill.
53	Ohmite Mfg. Co.	3635 Howard St. Skokie, Illinois
55	Centralab	900A E. Keefe Ave. Milwaukee, Wisc.
63	Transitron Electronic Corp.	168-182 Albion St. Wakefield, Mass.

Table 5-21. Supplier Code Index (Cont.)

Code No.	Name	Address
63	Transitron Electronic Corp.	168-182 Alibion St. Wakefield, Mass.
68	Delta Semiconductors Inc.	835 Production Place Newport Beach, Calif.
70	Nytronics, Inc.	550 Springfield Ave. Berkeley Heights, N. J.
72	Ferroxcube Corp. of America	E. Bridge Street Saugerties, N. Y.
73	Electra Mfg. Co.	4051 Broadway Kansas City, Mo.
74	Same as 25	
76	Same as 24	
77	Same as 24	
80	Same as 23	
81	Same as 20	
82	Elco Corporation	Willow Grove, Penn.
84	General Electric Co. Miniature Lamp Dept.	Nela Park Cleveland 12, Ohio
90	J. W. Miller Co.	5917 S. Main St. Low Angeles 3, Calif.
91	Stanwyck Winding Co.	137 Walsh Ave. Newburgh, N. Y.
95	Philco Corp.	Lansdale Division Lansdale, Penn.
96	Amperex Electronic Corp.	230 Duffy Ave. Hicksville, N. Y.
100	Same as 53	
106	Arrow-Hart and Hegeman Electric	103 Hawthorne St. Hartford, Conn.
113	Controls Co. of America	9555 Soreng Ave. Schiller Park, Ill.
138	Monitor Products, Inc.	815 Fremont Ave. South Pasadena, Calif.
141	Minneapolis-Honeywell Semiconductor Products	2747 4th Ave. South Minneapolis, Minn.
160	Magtrol, Inc.	241 Seneca Street Buffalo 4, N. Y.
161	West Coast Electrical Mfg. Co.	233 W. 116th Place Los Angeles 61, Calif.
162	Minneapolis-Honeywell Micro Switch Division	Chicago and Spring St. Freeport, Ill.
163	Eldema Corp.	1805 Belcroft Ave. El Monte, Calif.
164	Potter and Brumfield Div. of Amer. Machine and Foundry	1200 E. Broadway Princeton, Indiana
165	Electric Indicator Company	Camp Avenue Stanford, Conn.
166	General Instrument Co. Magne Head Division	3216 W. El Segundo Hawthorne, Calif.
167	Contract Tool Corp.	3820 Hoke Ave. Culver City, Calif.
176	Clarostat Mfg. Co. Inc.	Washington St. Dover, New Hampshire
185	Mepco Inc.	35 Abbet Ave. Morristown, N. J.
188	Aerovox Corp.	740 Belleville Ave. New Bedford, Mass.
189	Cornell-Dubilier	50 Paris Street Newark 1, N. J.
191	Dearborn Labs	Box 3431 Orlando, Florida
192	TRW Capacitor, Div.	112 W. 1st Street Ogallala, Nebraska
193	Electron Products	1962 Walker Ave. Monrovia, Calif.
202	Dickson Elect. Corp.	310 S. Wells Fargo Scottsdale, Arizona
225	National Transistor Div. ITT	500 Broadway Lawrence, Mass.
234	Key Resistor Corp.	321 W. Redondo Beach Blvd., Gardena, Calif.
269	International Rectifier	233 Kansas St. El Segundo, Calif.

SECTION VI
DRAWINGS

6-1 GENERAL

6-2 This section contains reference drawings useful in servicing and maintaining the MAGPAK Tape System. Included are installation drawings (figures 6-1 through 6-3), logic diagrams for both Model 9446 and Model 9448 (figures 6-4 and 6-5), power distribution diagrams (figure 6-6), and schematic diagrams (figures 6-7 through 6-30).

6-3. To aid in finding signal sources on the logic diagrams, two signal-location charts (tables 6-1 and 6-2) are included. Table 6-1 shows signal locations for figures 6-4, and table 6-2 shows them for figure 6-5.

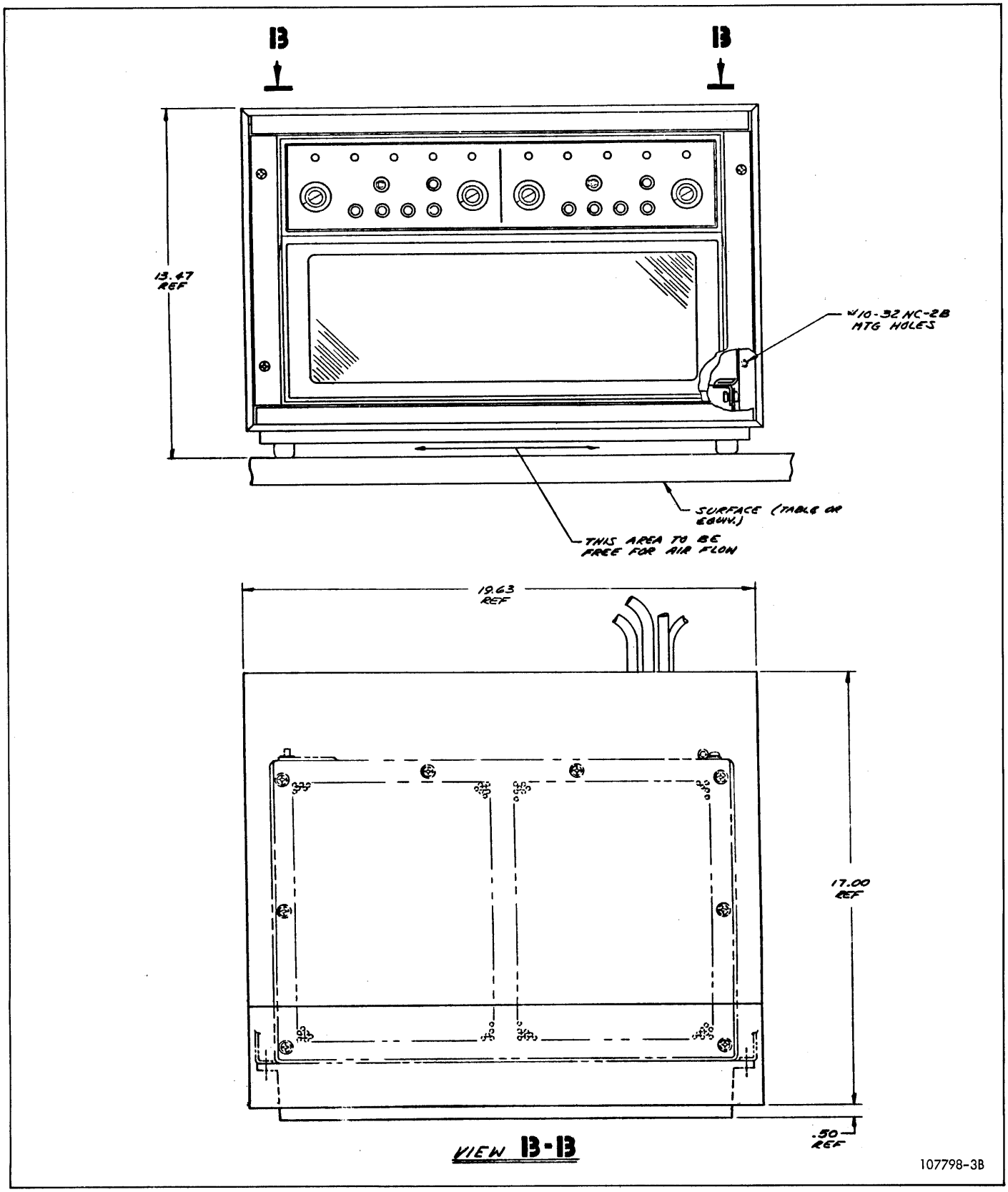


Figure 6-1. Model 9446 Installation, Table-Mounted

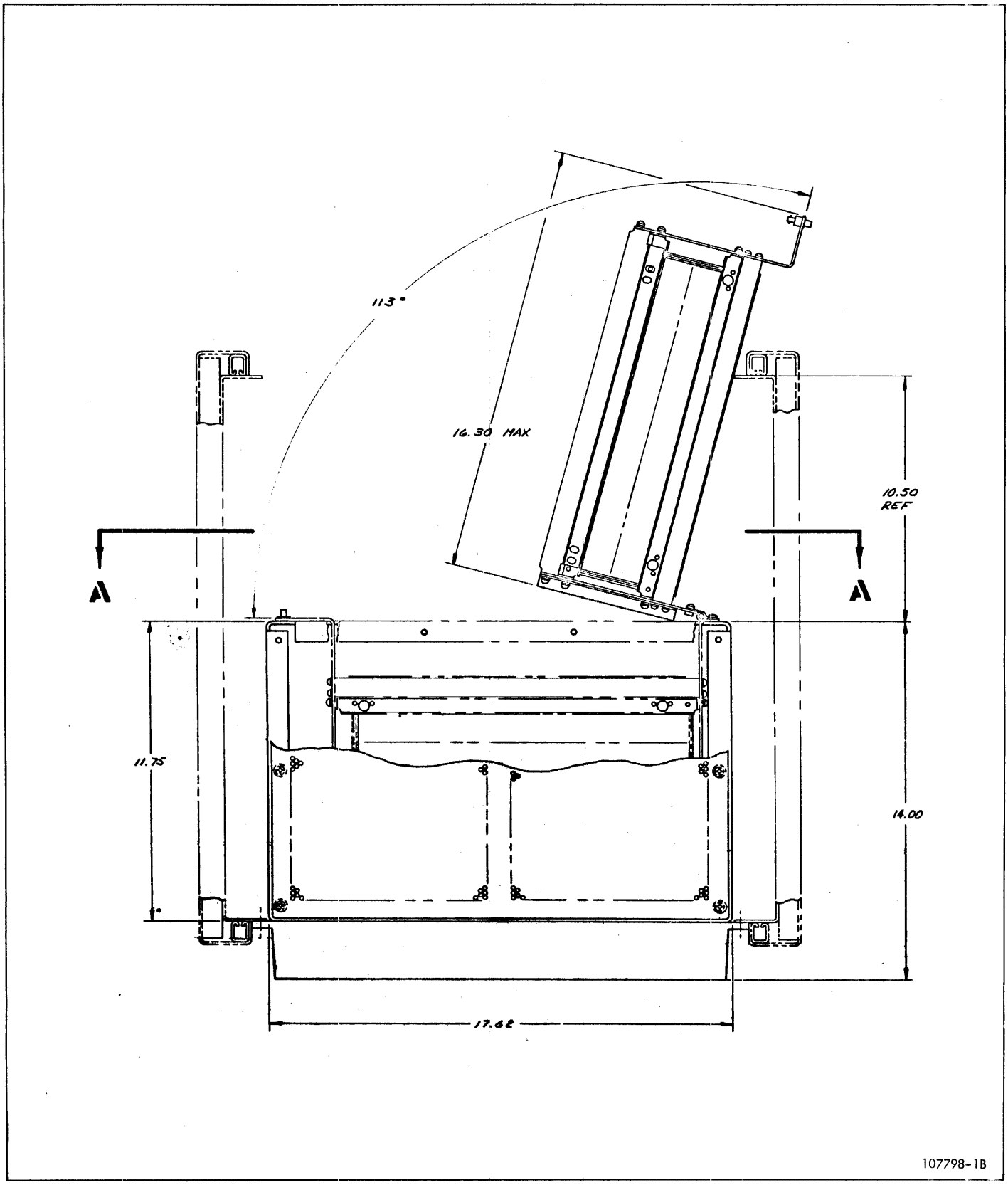


Figure 6-2. Model 9446 Installation, Rack-Mounted (Sheet 1 of 2)

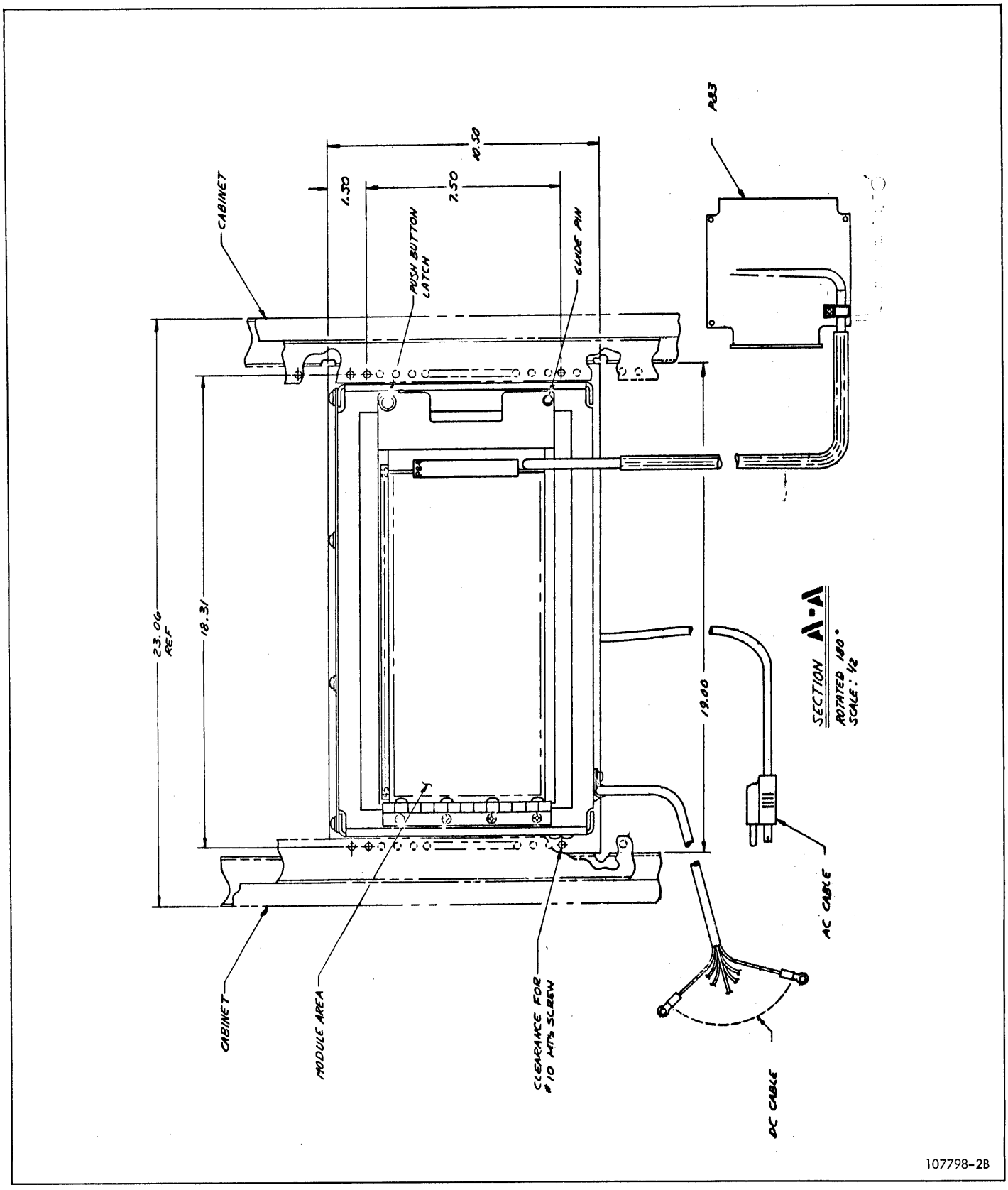


Figure 6-2. Model 9446 Installation, Rack-Mounted (Sheet 2 of 2)

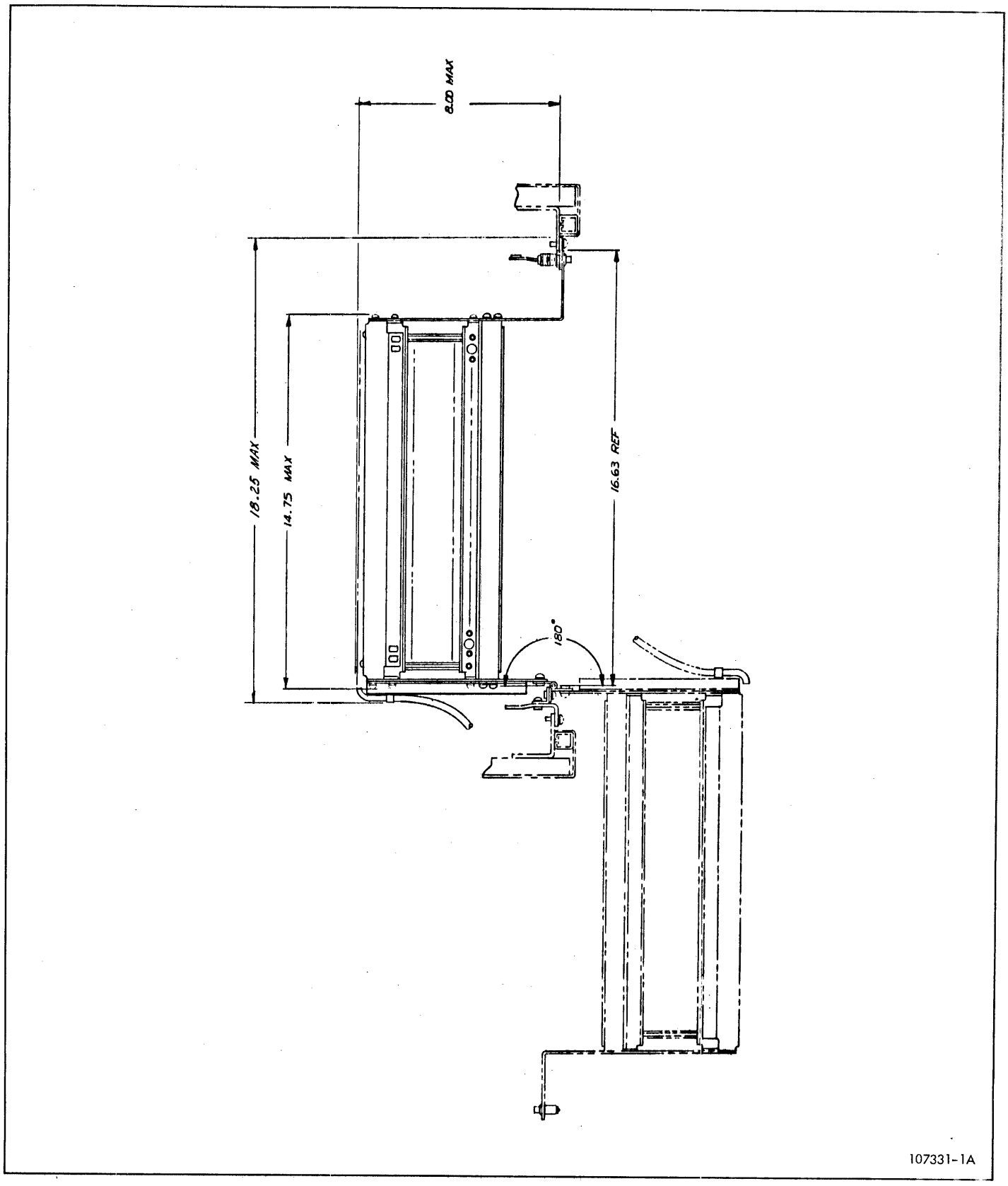


Figure 6-3. Model 9448 Installation (Sheet 1 of 2)

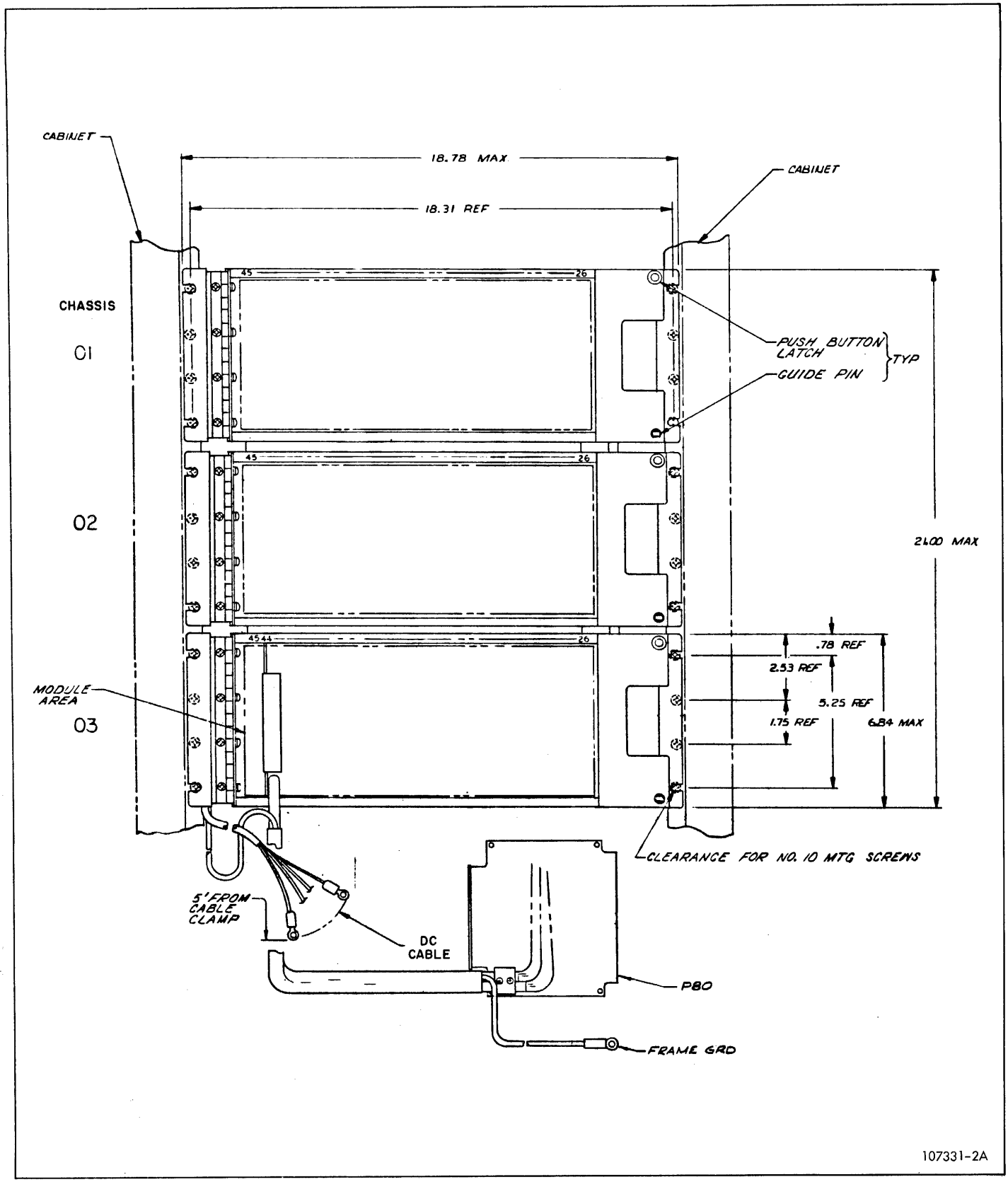


Figure 6-3. Model 9448 Installation (Sheet 2 of 2)

Table 6-1. Model 9446 Signal Location Chart (for use with figure 6-4)

Signal	Fig. 6-4 Sheet No.	Signal	Fig. 6-4 Sheet No.	Signal	Fig. 6-4 Sheet No.
AANS	1	ETK2	2	LWN2	4
$\overline{\text{AANS}}$	1, 2	ETL	3, 7	MAN1	1
AUT	3, 7	ETL1	3	MAN2	2
AUT1	3, 4, 5	ETL2	3	PLP1	3
AUT2	4	ETT1	1	PLP2	3
BOR	7	ETT2	2	RDAS	5
$\overline{\text{BOTS}}$	1, 2	FPD1	1	RDA1	1, 3
BOT1	1, 3, 6	FPD2	2	RDA2	2, 3
$\overline{\text{BOT1}}$	1, 3	FPN1	1	RDD1	5
BOT2	2, 3, 6	FPN2	2	$\overline{\text{RDD1}}$	5
$\overline{\text{BOT2}}$	3	FWD1	1	RDD2	5
BRK1	1	FWD2	2	$\overline{\text{RDD2}}$	5
BRK2	2	LES1	4	RDK	5, 7
BTA	7	LES2	4	RDN1	5
BTK	7	$\overline{\text{LND1}}$	3	RDN2	5
BTK1	1	LND2	3	$\overline{\text{RDN2}}$	5
BTK2	2	$\overline{\text{LND2}}$	3	RDR	5, 7
BTL	7	LRD1	5	$\overline{\text{RDYS}}$	1, 2
BTL1	3	LRD2	5	RDY1	1, 3
BTL2	3	LRN1	5	RDY2	2, 3
CHSB	3, 4, 5	LRN2	5	REV1	1
$\overline{\text{CHSB}}$	3, 4, 5	LTDB	3	REV2	2
DATA	4, 5	$\overline{\text{LTDB}}$	3	REWM	1, 2
$\overline{\text{DATA}}$	4	LTD1	1, 3	REW1	1
EOR	7	$\overline{\text{LTD1}}$	1, 3	REW2	2
EOTS	2	LTD2	2	RHS	7
$\overline{\text{EOTS}}$	1	LTD2	3	RNG	5, 7
EOT1	1	LTNB	3	RNU	5, 7
$\overline{\text{EOT1}}$	1, 3	LTNB	3	SELP	4
EOT2	2	LTN1	1, 3	SELS	4
$\overline{\text{EOT2}}$	3	LTN1	1, 3	SEL1	1, 4, 5
ETA	7	LTN2	2	SEL2	2, 4, 5
ETA1	1	LTN2	3	STOP	1, 2, 3, 4
ETA2	2	LWD1	4	$\overline{\text{STOP}}$	3
ETK	7	LWD2	4	S12T	3
ETK1	1	LWN1	4	TFPS	1, 2

Table 6-1. Model 9446 Signal Location Chart (for use with figure 6-4) (Cont.)

Signal	Fig. 6-4 Sheet No.	Signal	Fig. 6-4 Sheet No.	Signal	Fig. 6-4 Sheet No.
$\overline{\text{TFPS}}$	1	TSB2	2, 3, 4	WDG1	4
TFP1	1	$\overline{\text{TSB2}}$	4	WDG2	4
TFP2	2	T12S	1, 2	WDW1	4
TSA1	1, 4	WED1	4	WDW2	4
$\overline{\text{TSA1}}$	1, 4	WED2	4	WNB1	4
TSA2	2, 4	WEN1	4	WNB2	4
$\overline{\text{TSA2}}$	4	WEN2	4	WNY1	4
TSB1	1, 3, 4	WDAS	4	WNY2	4
$\overline{\text{TSB1}}$	1, 4	$\overline{\text{WDAS}}$	4	WRTS	4

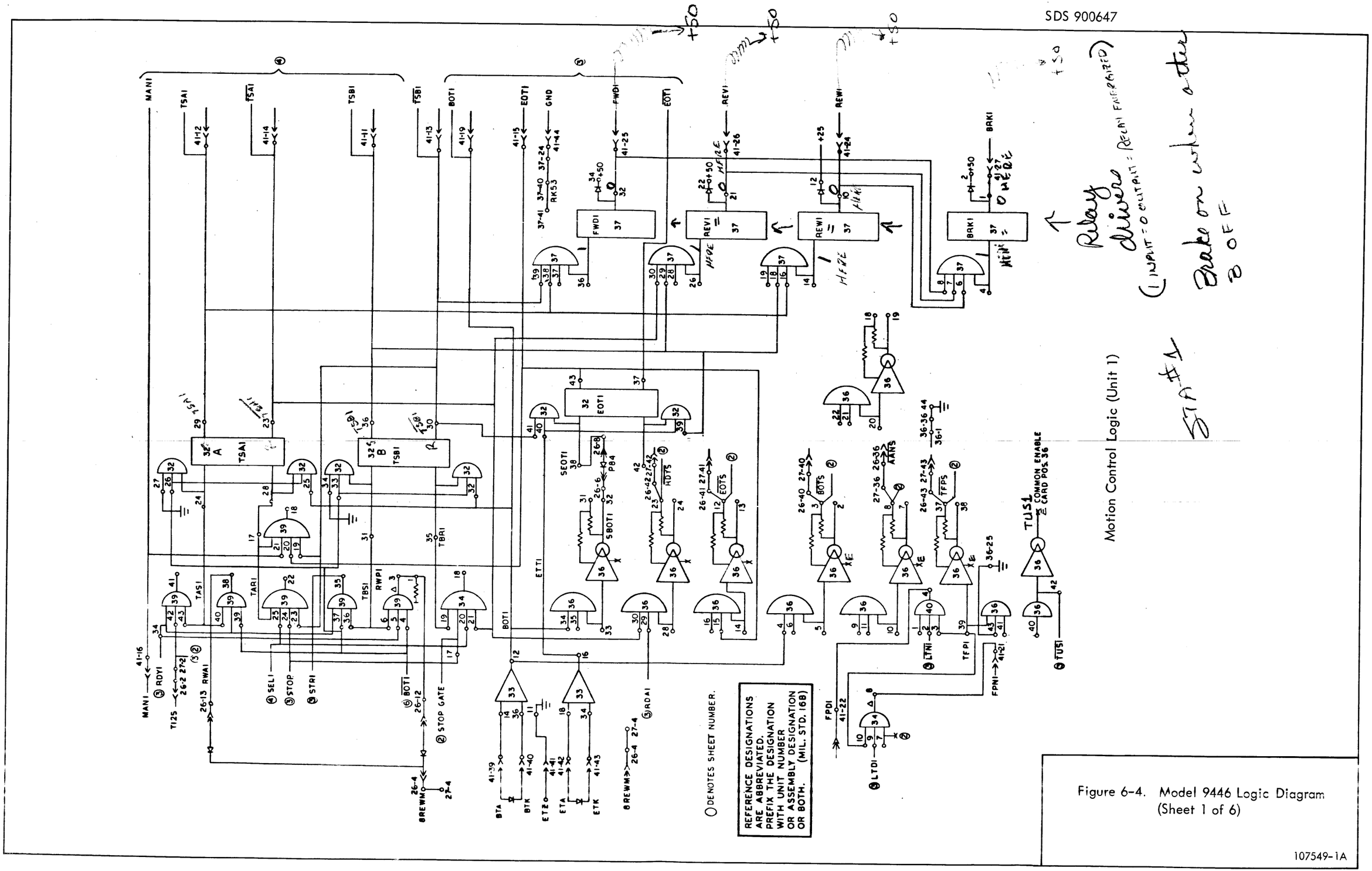


Figure 6-4. Model 9446 Logic Diagram (Sheet 1 of 6)

107549-1A

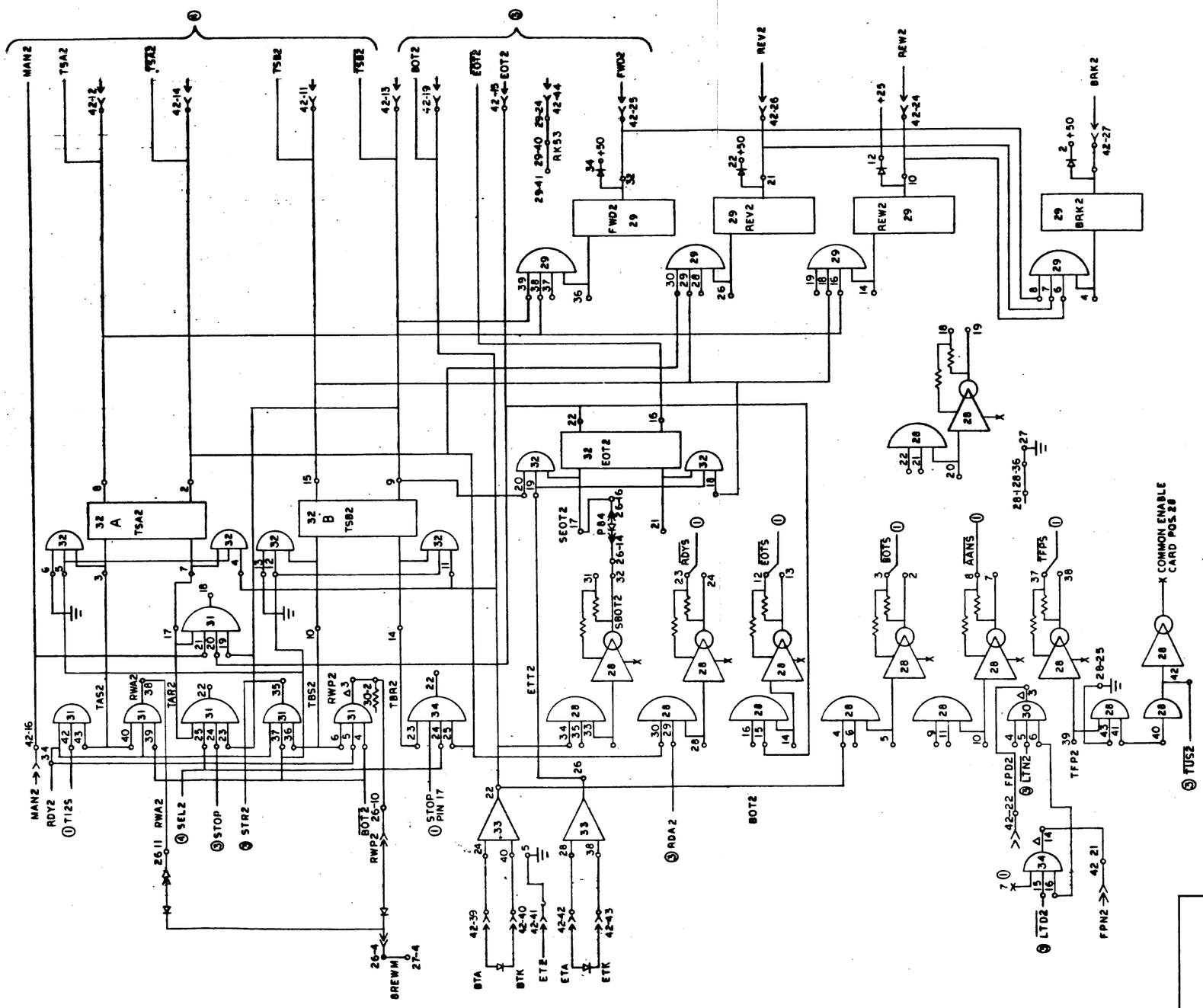


Figure 6-4. Model 9446 Logic Diagram (Sheet 2 of 6)

107549-2A

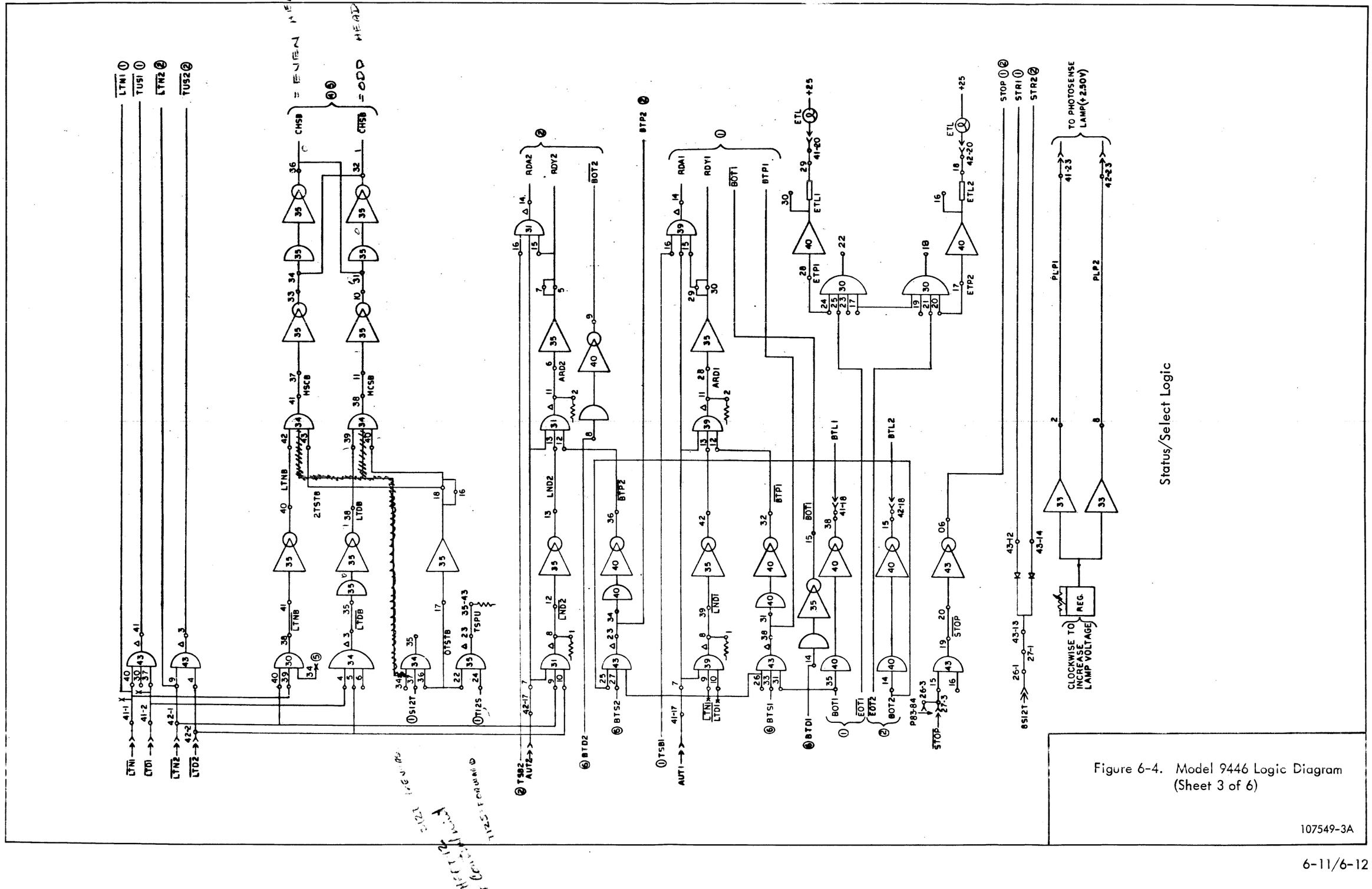


Figure 6-4. Model 9446 Logic Diagram (Sheet 3 of 6)

107549-3A

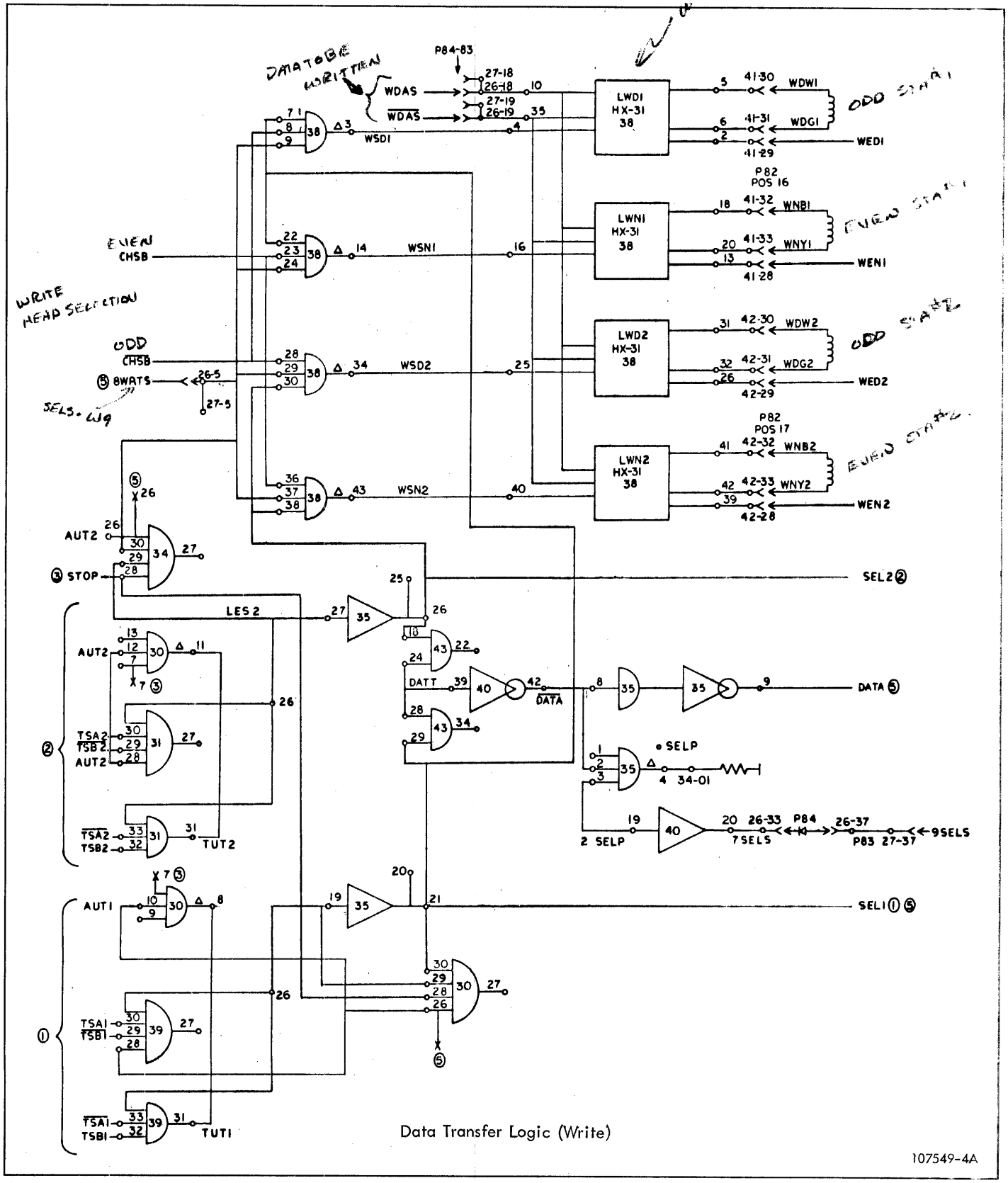
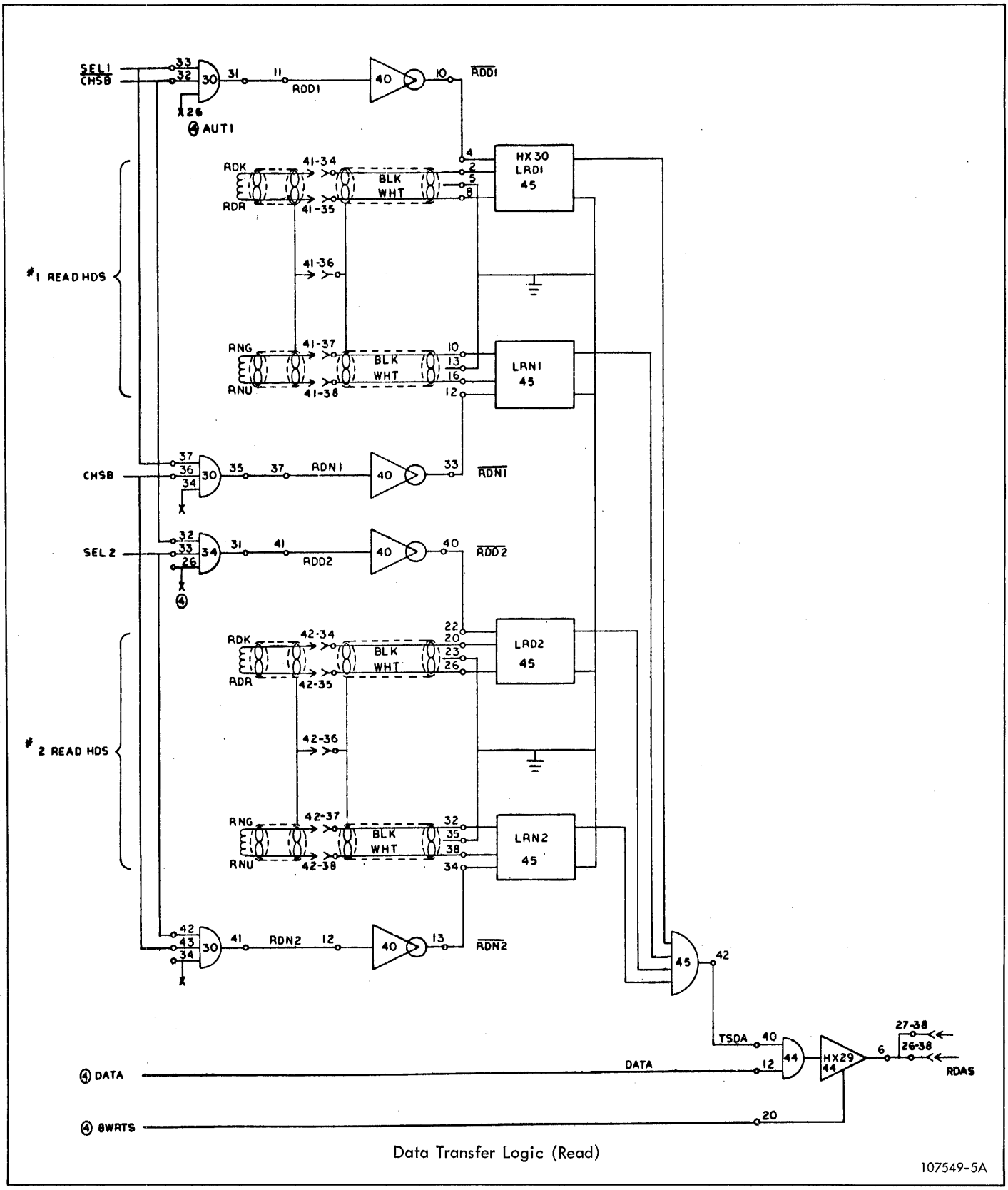


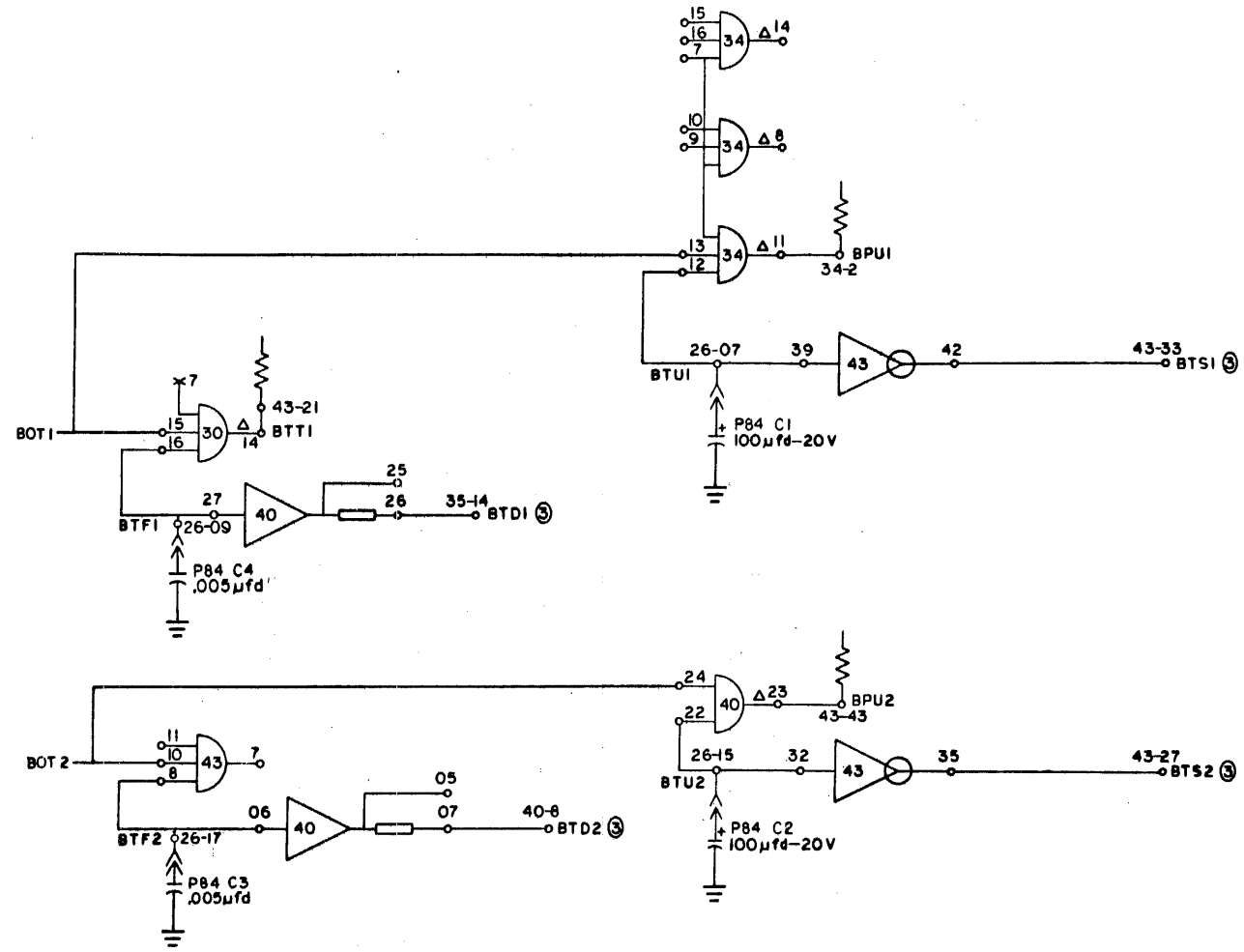
Figure 6-4. Model 9446 Logic Diagram (Sheet 4 of 6)



Data Transfer Logic (Read)

107549-5A

Figure 6-4. Model 9446 Logic Diagram (Sheet 5 of 6)



Delayed BOT Logic

107549-6A

Figure 6-4. Model 9446 Logic Diagram (Sheet 6 of 6)

Table 6-2. Model 9448 Signal Location Chart (for use with figure 6-5)

Signal	Fig. 6-5 Sheet No.	Signal	Fig. 6-5 Sheet No.	Signal	Fig. 6-5 Sheet No.
AANS	12	CUG	9	RC	3
BOTS	12	CURD	8	RCP	4
BUC	14	CUS 7	11	RCRG	4
BUC 9	5	CUWD	8	RDA	3
CBG	6	C12M	11	RDYS	12
CECF	10	C12	14	REWM	12
CERF	11	C13	14	RF	3
CETF	10	C14	14	RG	3
CFMF	10	C15	14	ROO1	3
CHROO	6	C16	14	ROO2	3
CHRO1	6	C170	14	RP	14
CHRO2	6	C21	14	RSA	4
CHRO2	6	C22	14	RSAB	5
CHRO3	6	C23	14	RSA3	3
CHRO4	6	ECM	5	RSB	4
CHRO5	6	EOTS	12	RSC	4
CHRO6	6	FC	1	RSC3	4
CNTL	12	GDA 4	13	RSD	4
CSA	8	HRG	6	RSE	4
CSB	8	HROO	6	RSF	4
CSC	8	HRO1	7	RSF3	3
CSG	9	HRO2	7	R1	14
CSOA	9	HRO3	7	R2	14
CSRF	11	HRO4	7	R3	14
CSO	9	HRO5	7	R4	14
CS1	9	HRO6	7	R5	14
CS2	9	IHGD	8	R6	14
CS3	9	IOC	14	SELS	10
CS4	9	IOC 9	5	SFG	6
CS5	9	LLT6	12	SPG	6
CS6	9	LLT7	12	SRG	6
CS7	9	MTG	5	STOP	12
CS13	9	Q2	14	STRT	12
CS27	9	Q29	5	S12T	12
CS56	9	RABC	5	S10	13
CUFF	11	RAB3	3	TEST	4

Table 6-2. Model 9448 Signal Location Chart (for use with figure 6-5) (Cont.)

Signal	Fig. 6-5 Sheet No.	Signal	Fig. 6-5 Sheet No.	Signal	Fig. 6-5 Sheet No.
TFPS	12	WGO1	2	W10	14
T12S	12	WHS	5	W11	14
WCA	1	WSA	2	W119	5
WCB	1	WSB	2	ZW1	5
WCC	1	WSC	2	ZW2	5
WCD	1	W9MO	8	ZW3	5
WCPO	1	WTRD	8	ZW4	5
WCP1	1	WO	14	ZW5	5
WDAS	2	W5	14	ZW6	5
WES	5	W6	14	ZW7	5
WF	2	W9	14		

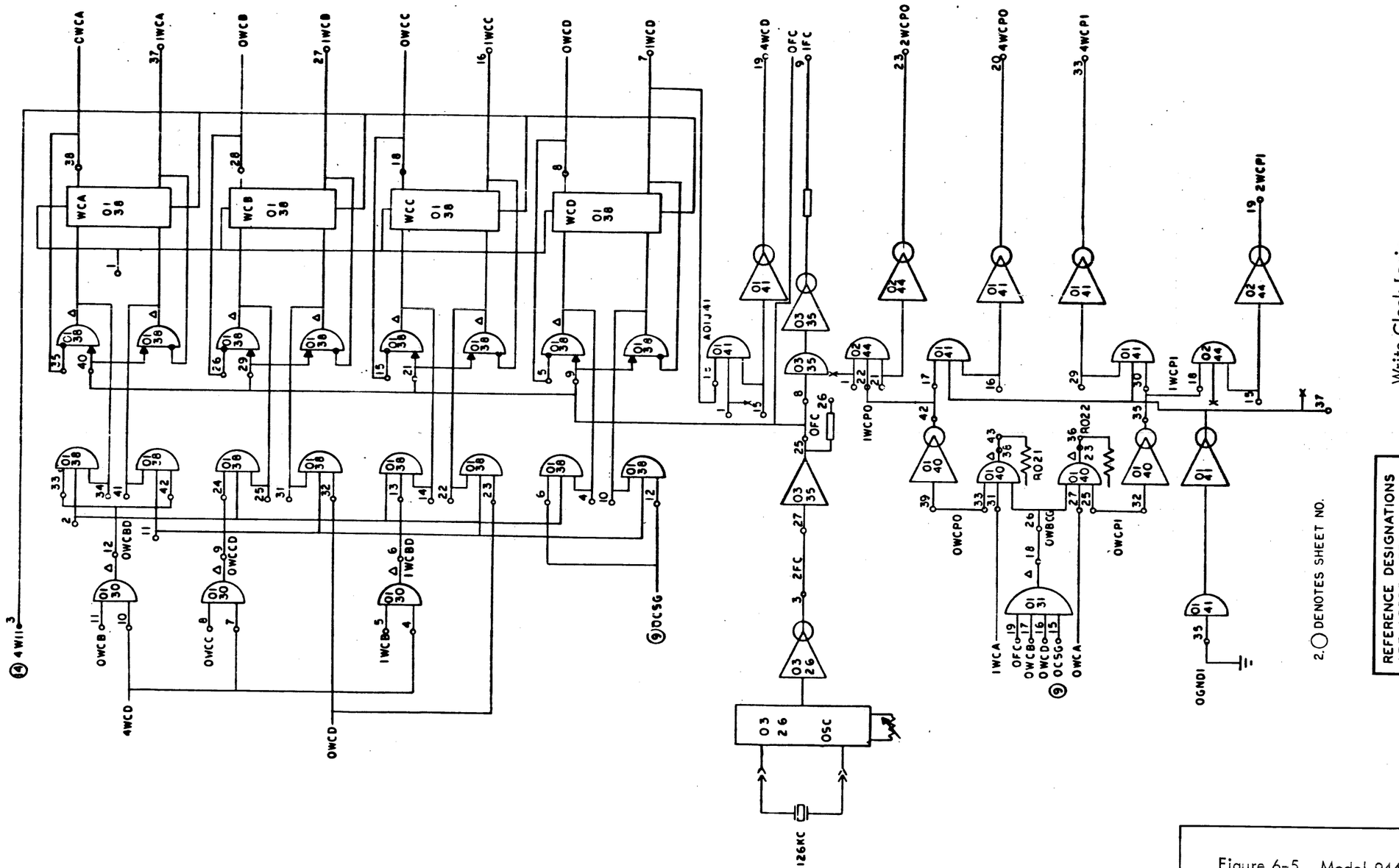


Figure 6-5. Model 9448 Logic Diagram (Sheet 1 of 14)

107548-1B

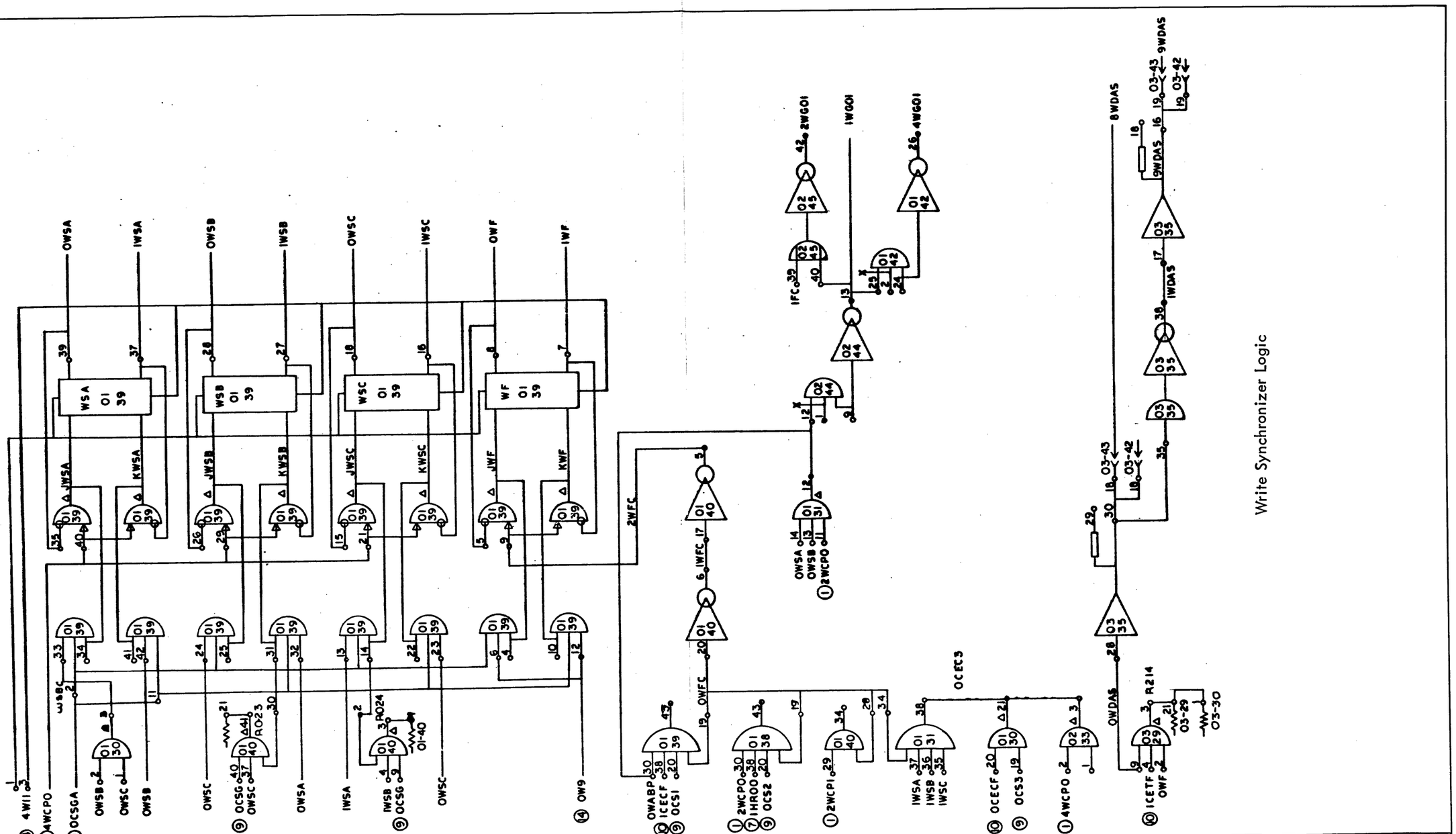


Figure 6-5. Model 9448 Logic Diagram (Sheet 2 of 14)

107548-2A

Read Decoder Logic

Figure 6-5. Model 9448 Logic Diagram
(Sheet 3 of 14)

107548-3B

Read Synchronizer Logic

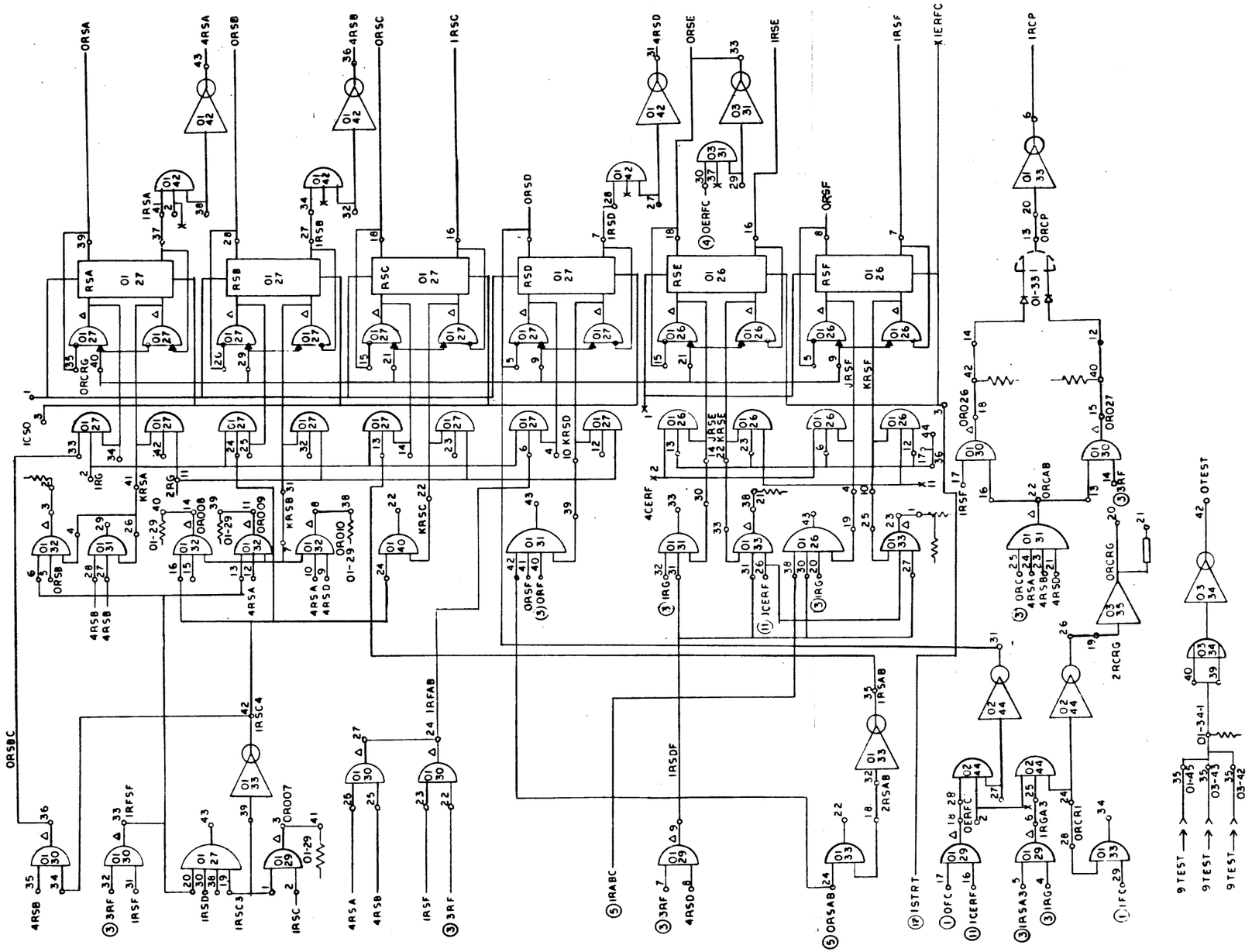


Figure 6-5. Model 9448 Logic Diagram (Sheet 4 of 14)

107548-4C

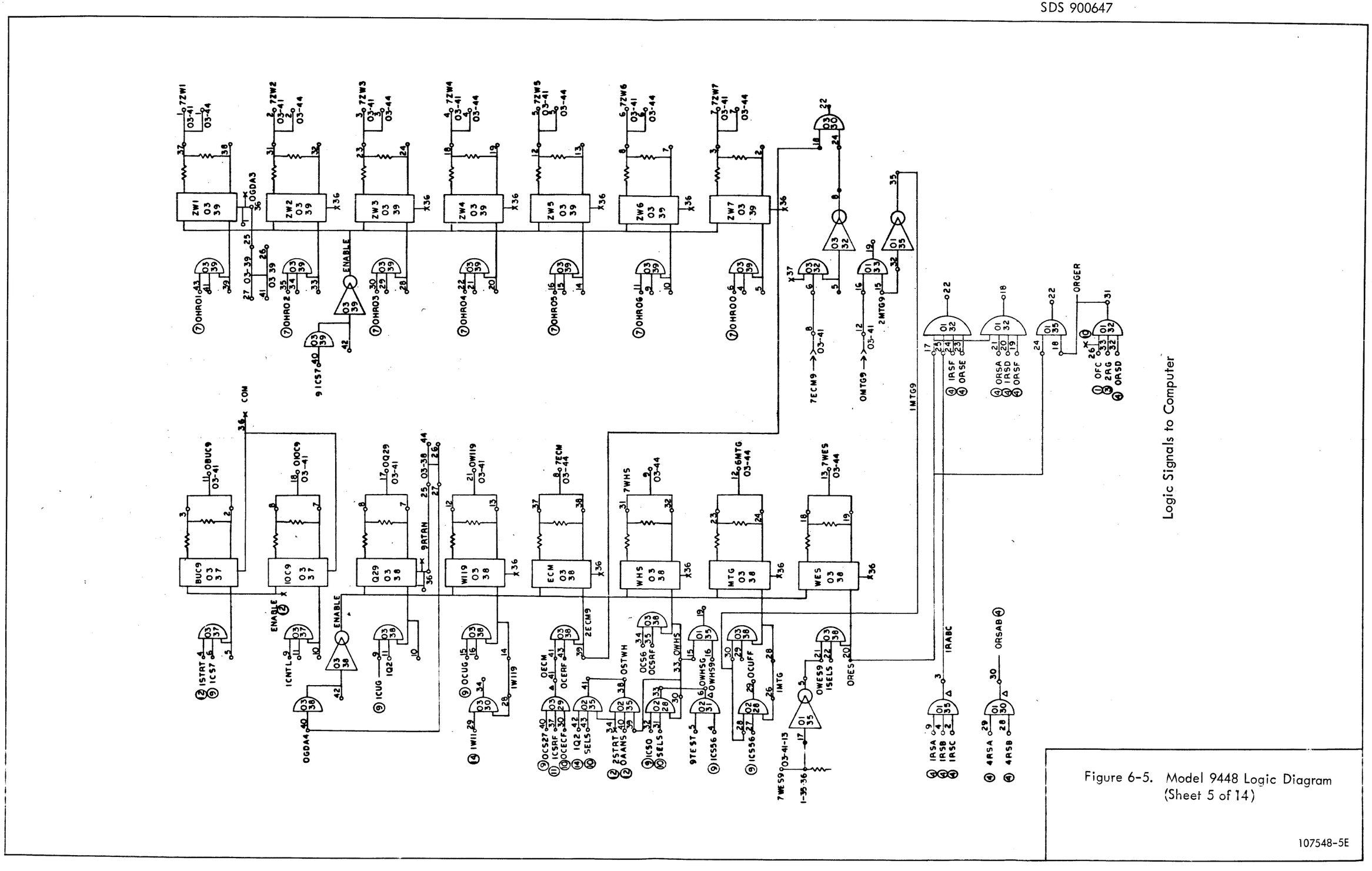
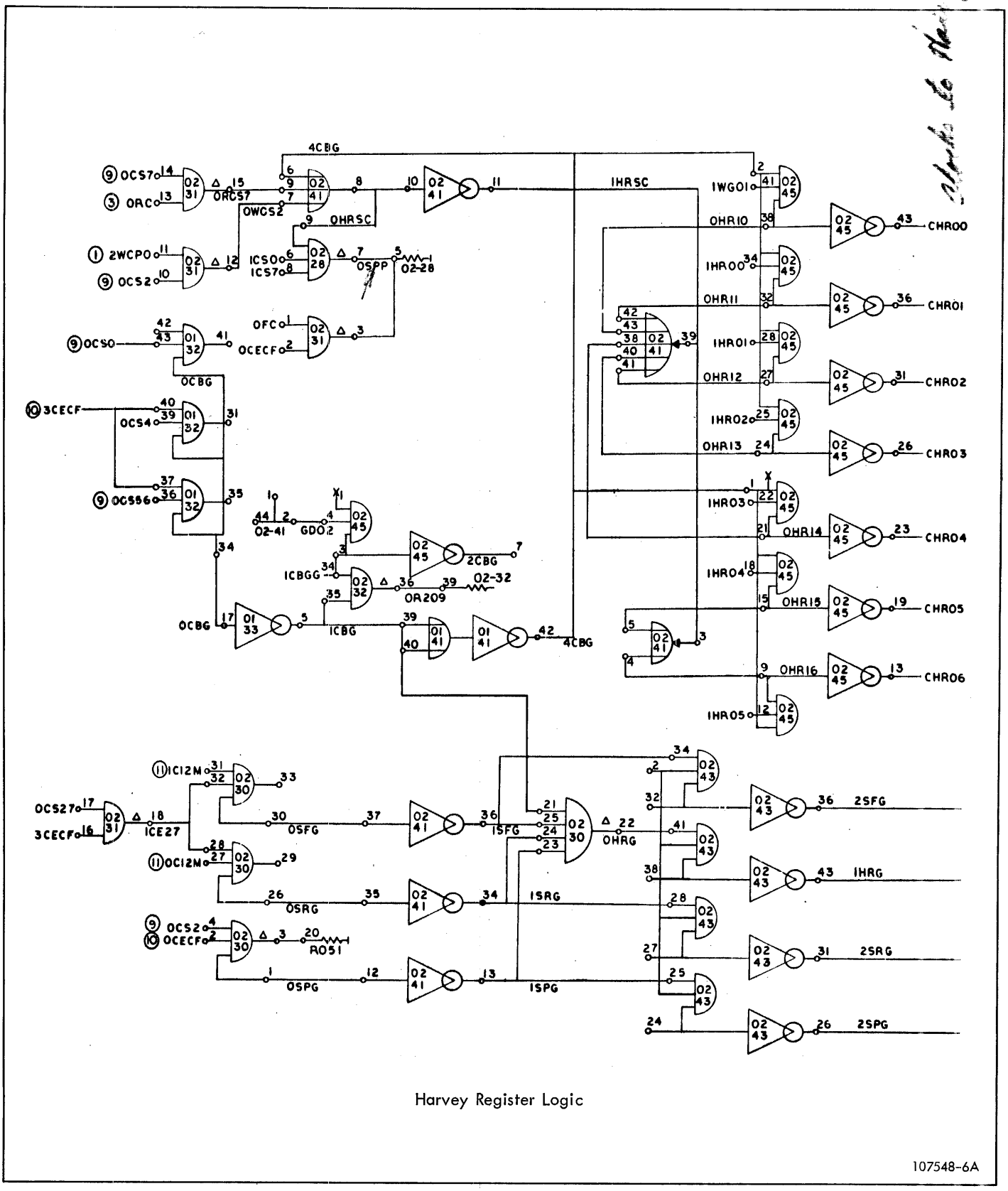


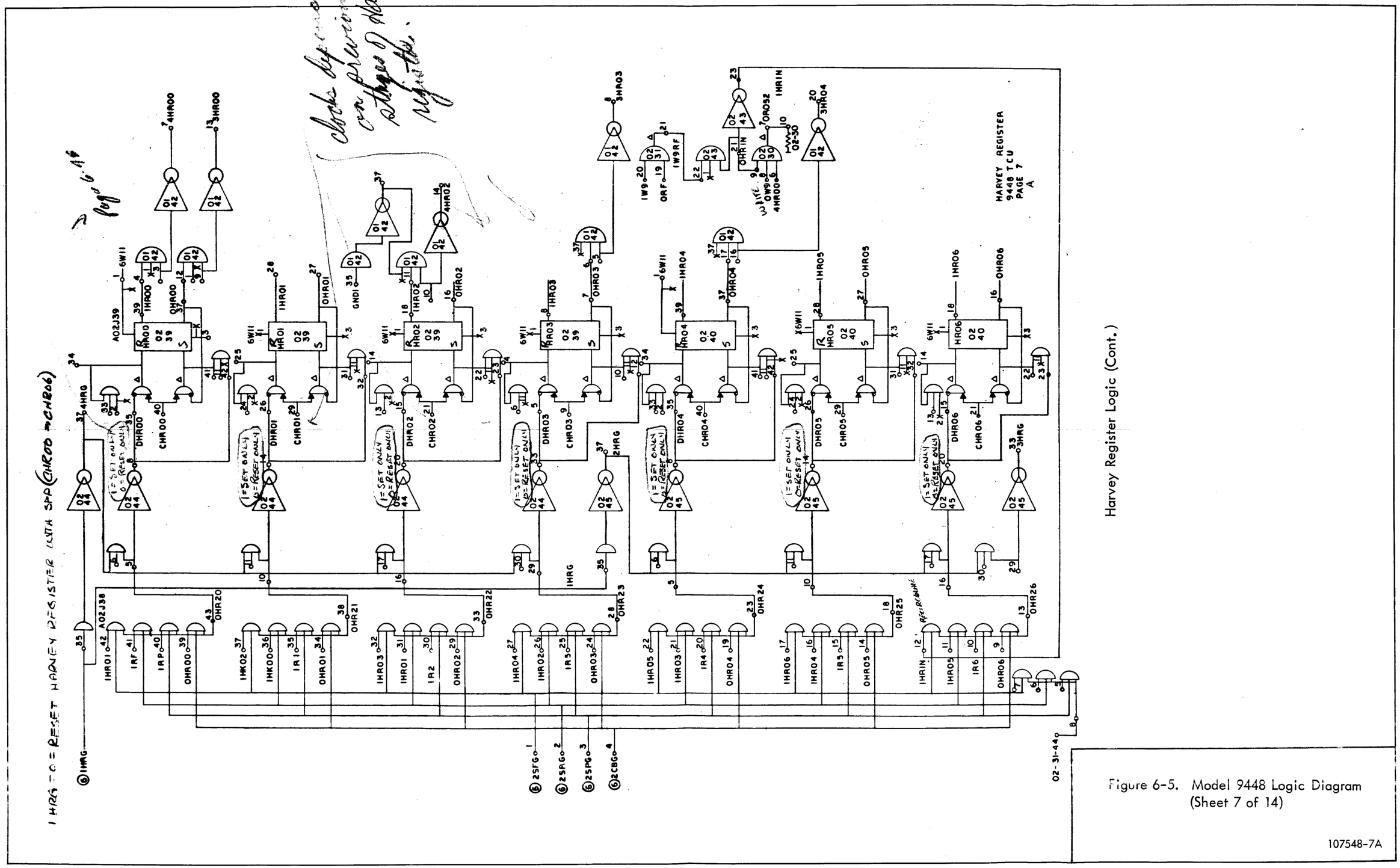
Figure 6-5. Model 9448 Logic Diagram (Sheet 5 of 14)

107548-5E



Harvey Register Logic

Figure 6-5. Model 9448 Logic Diagram (Sheet 6 of 14)



Harvey Register Logic (Cont.)

Figure 6-5. Model 9448 Logic Diagram (Sheet 7 of 14)

107548-7A

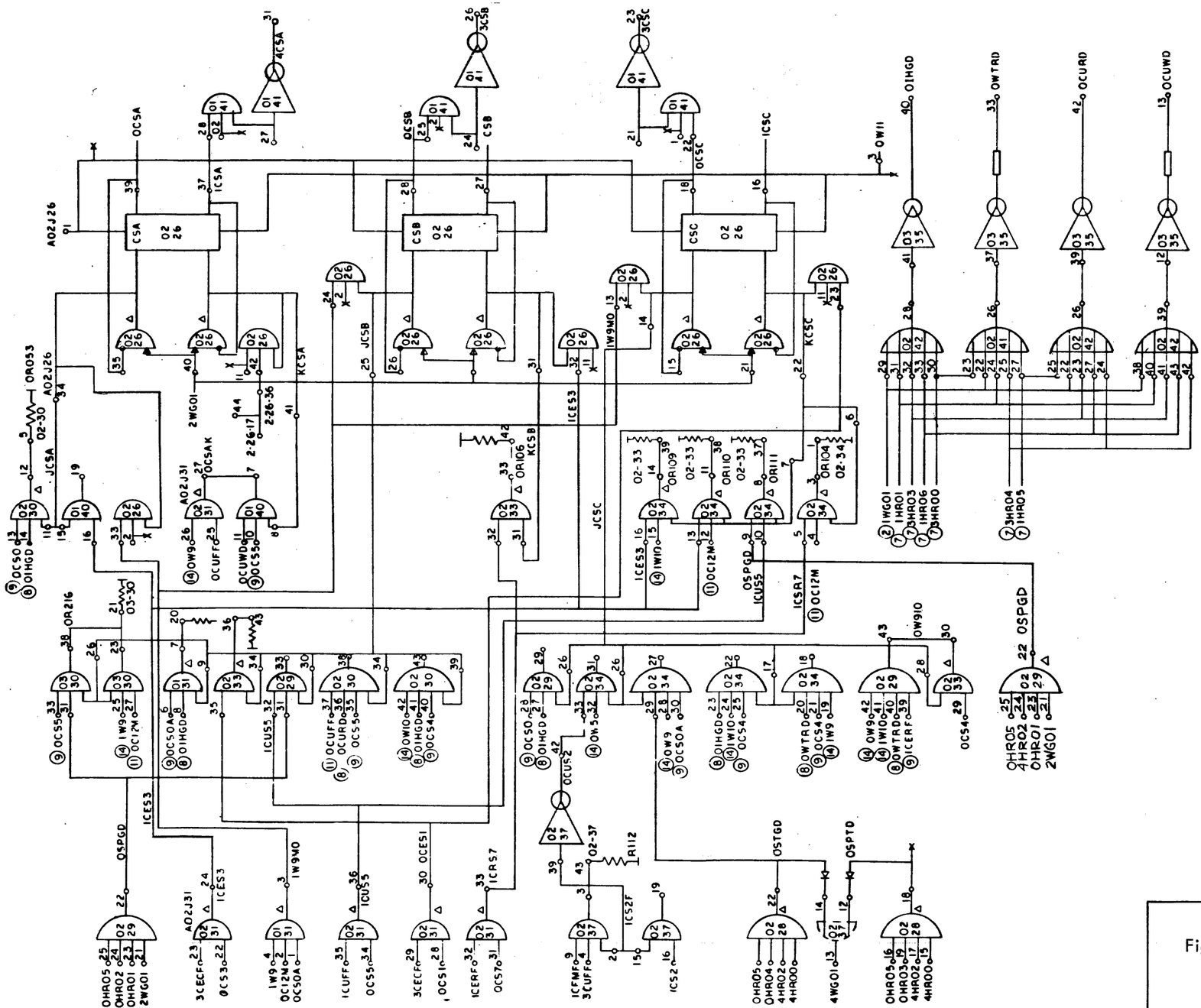


Figure 6-5. Model 9448 Logic Diagram
(Sheet 8 of 14)

107548-8A

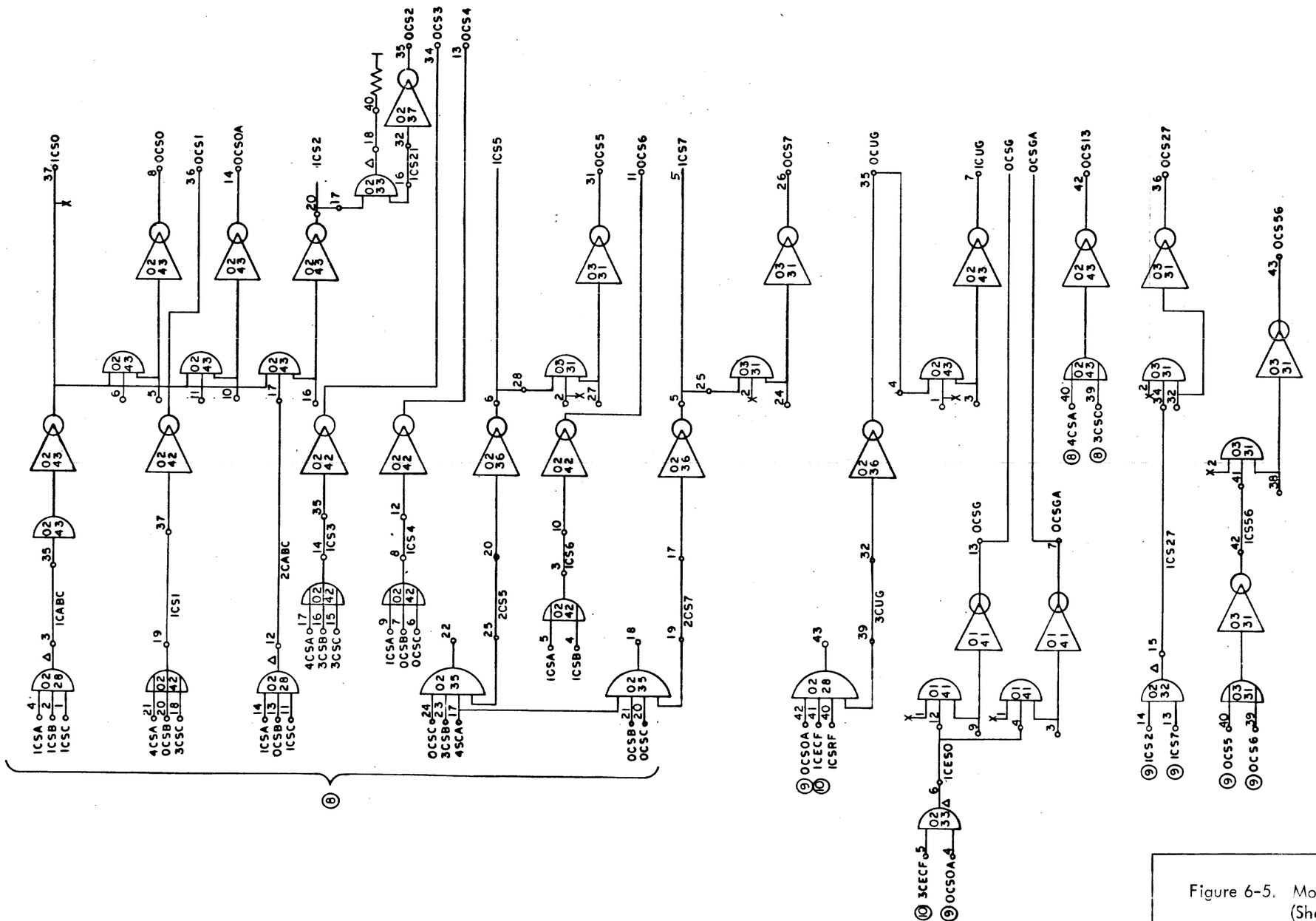


Figure 6-5. Model 9448 Logic Diagram (Sheet 9 of 14)

107548-9A

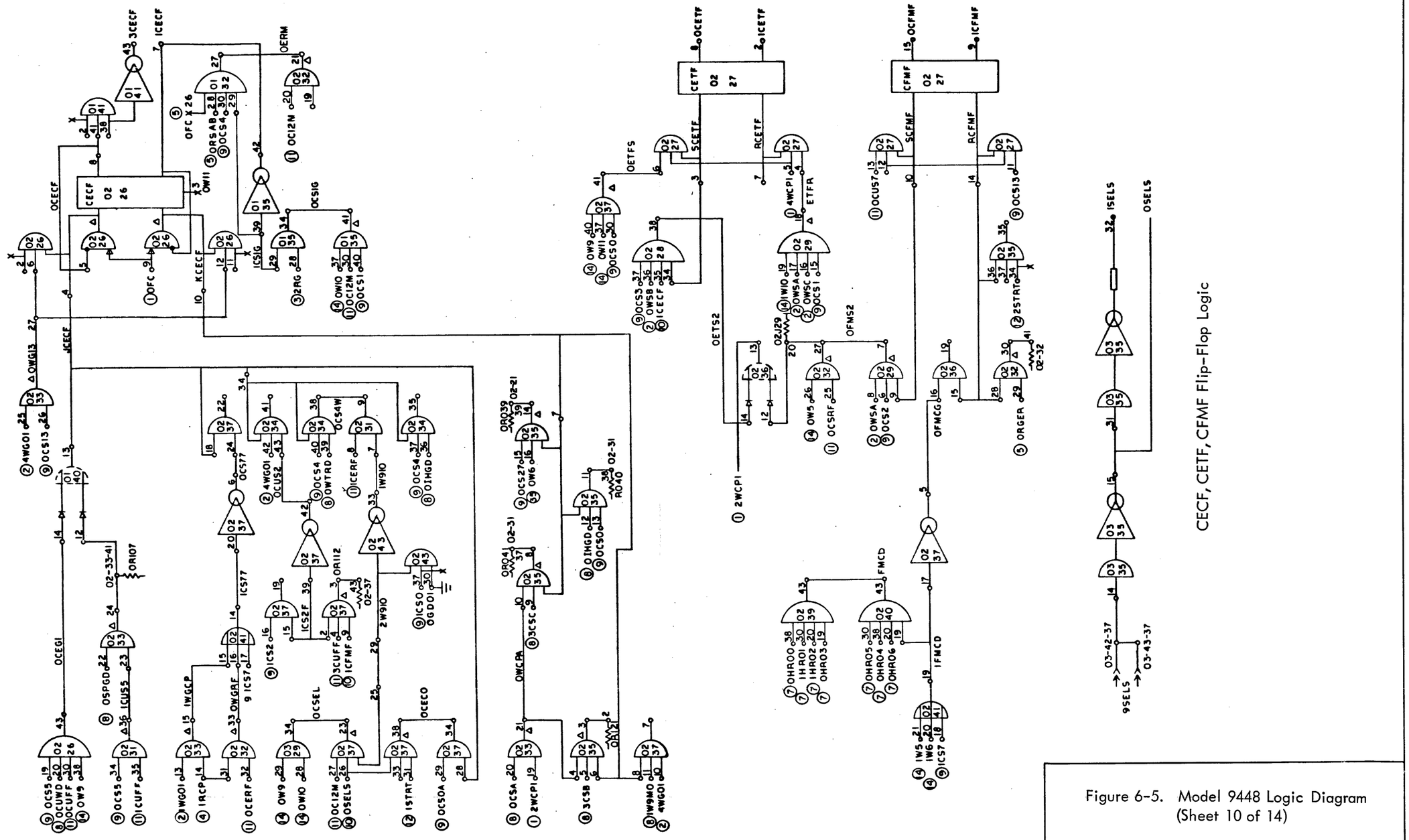


Figure 6-5. Model 9448 Logic Diagram
(Sheet 10 of 14)

107548-10D

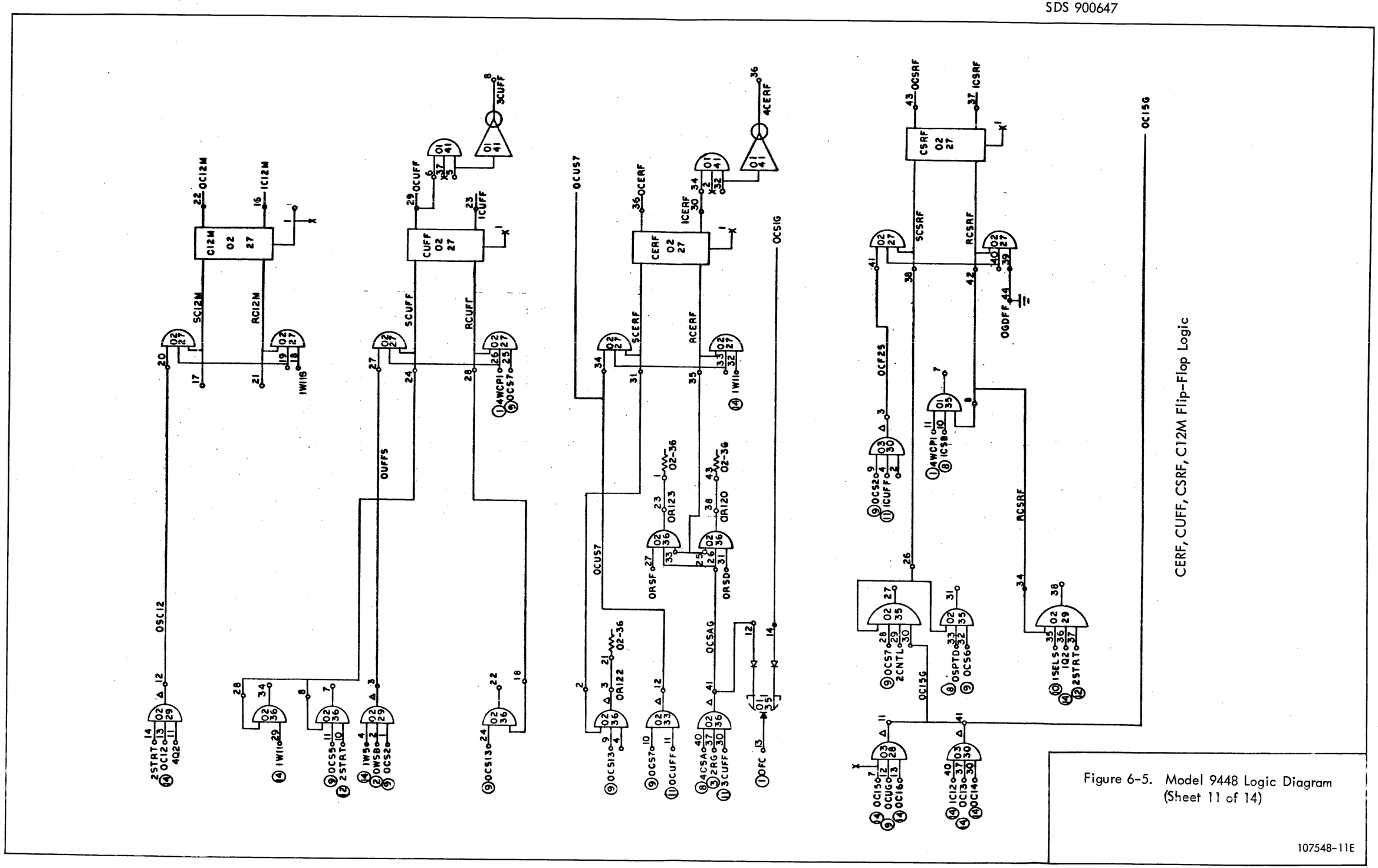


Figure 6-5. Model 9448 Logic Diagram
(Sheet 11 of 14)

107548-11E

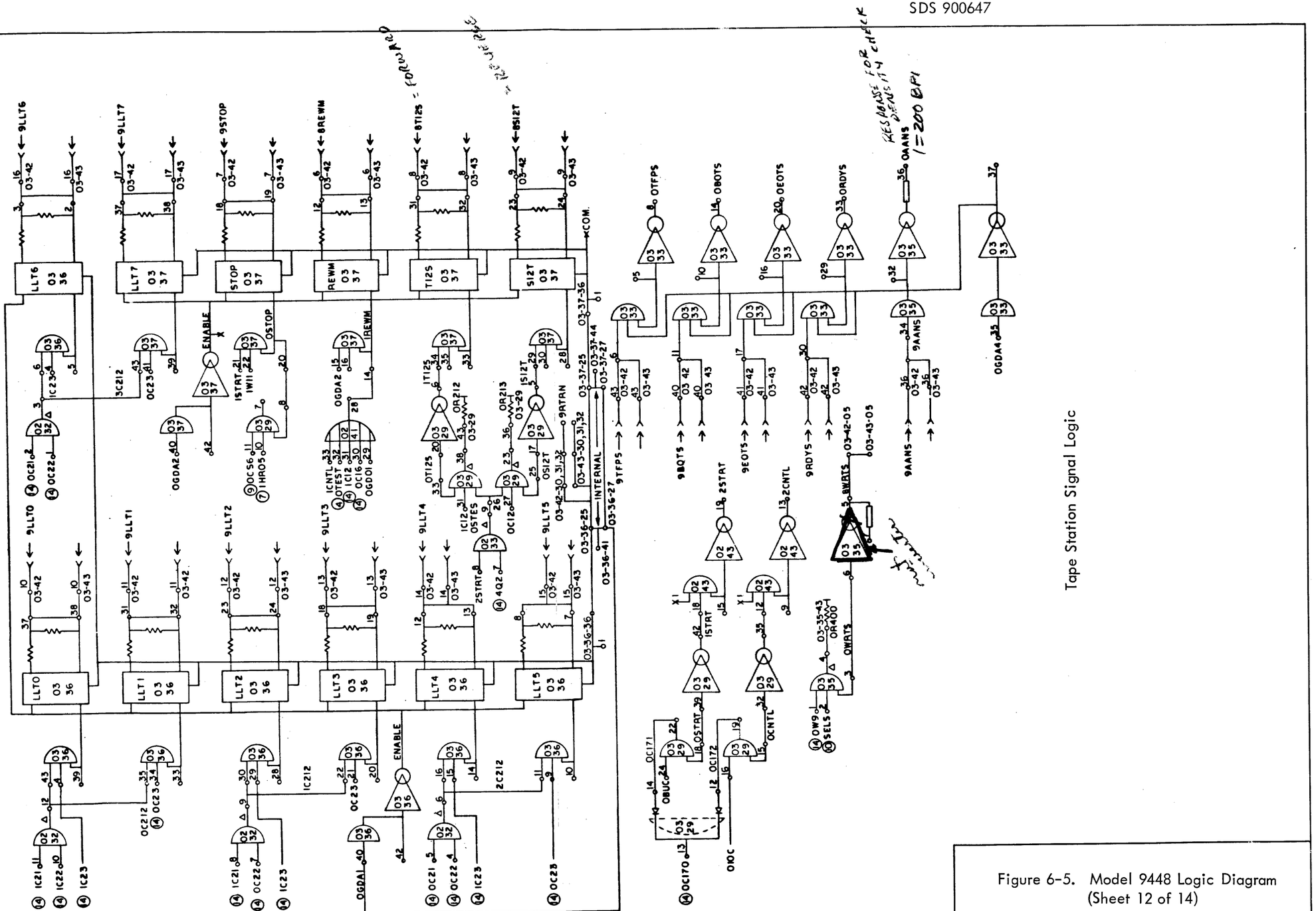


Figure 6-5. Model 9448 Logic Diagram
(Sheet 12 of 14)

107548-12A

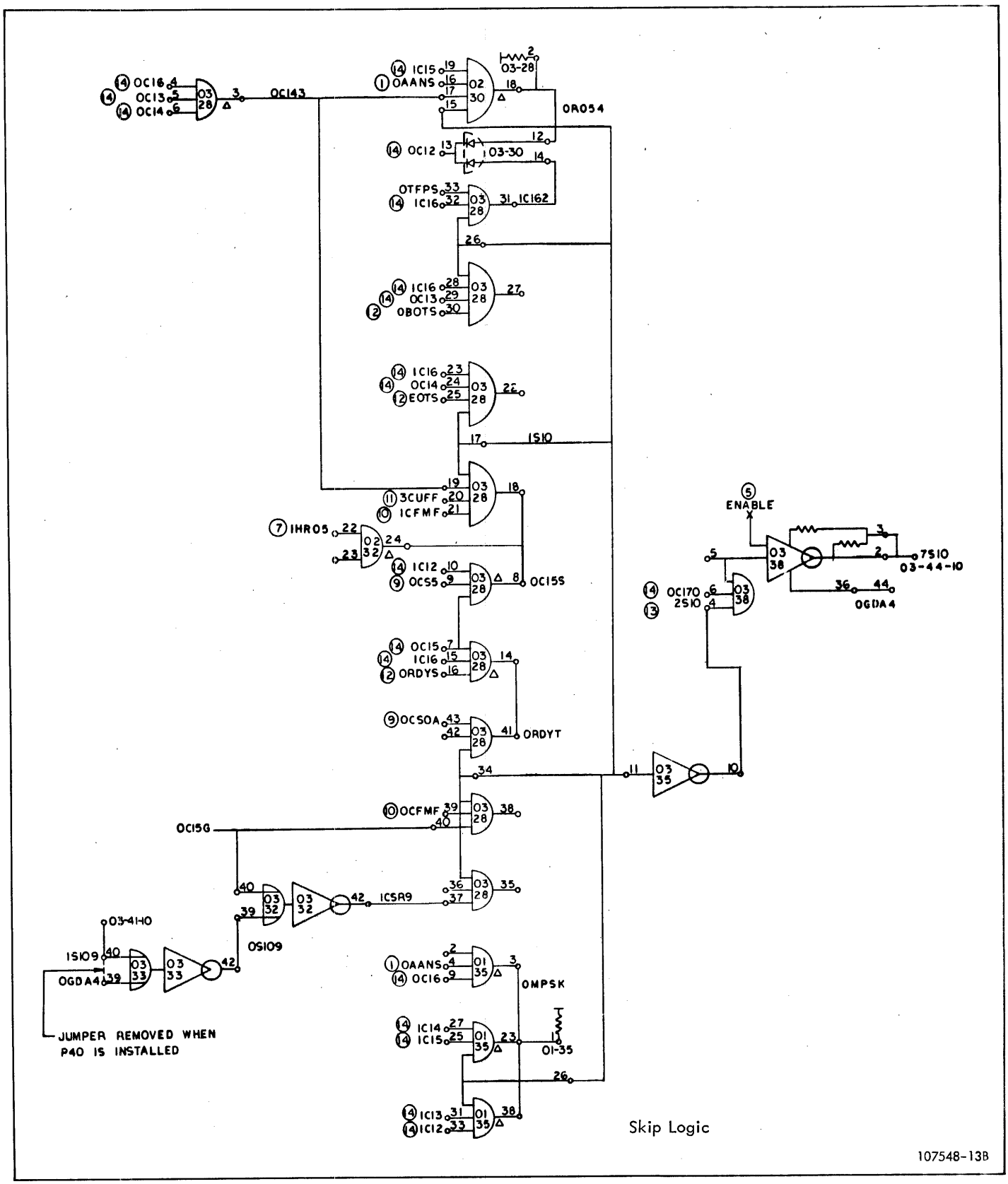


Figure 6-5. Model 9448 Logic Diagram (Sheet 13 of 14)

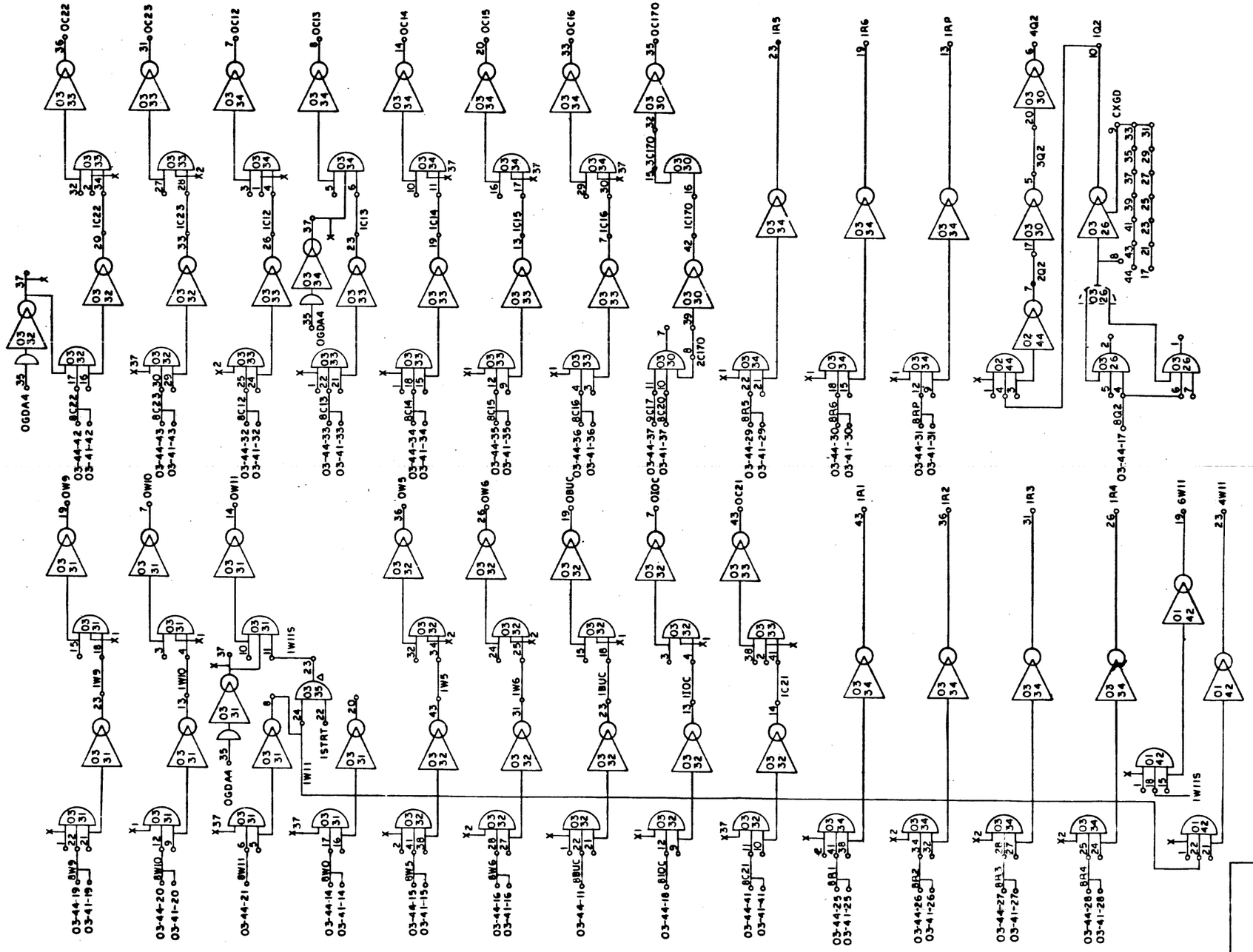
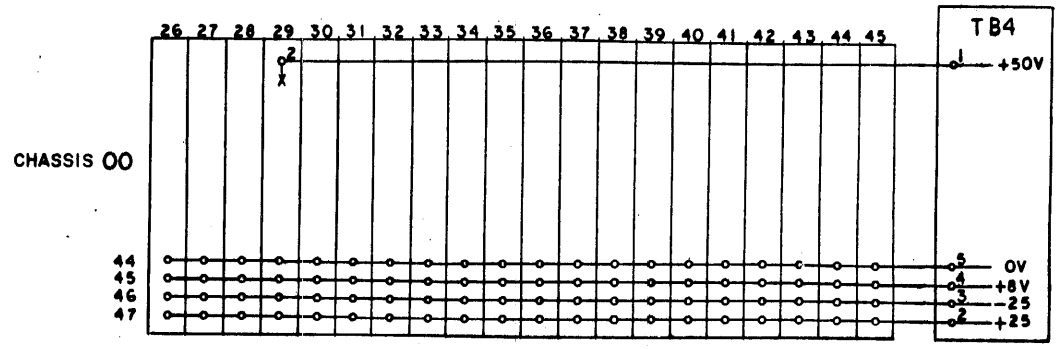


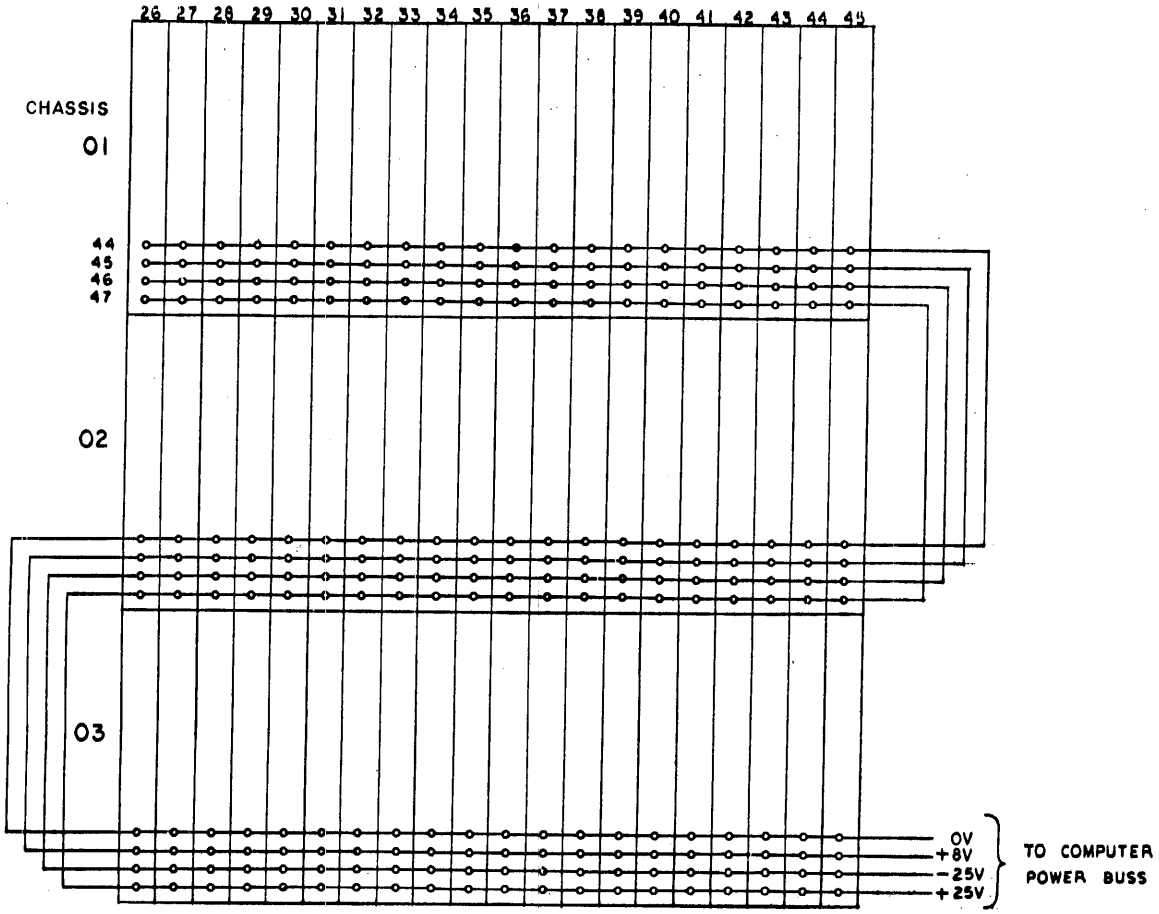
Figure 6-5. Model 9448 Logic Diagram
(Sheet 14 of 14)

107548-14E



Model 9446 Module Chassis Power Distribution

107549-10E



Model 9448 Module Chassis Power Distribution

107548-19

Figure 6-6. Module Chassis Power Distribution (Models 9446 and 9488)

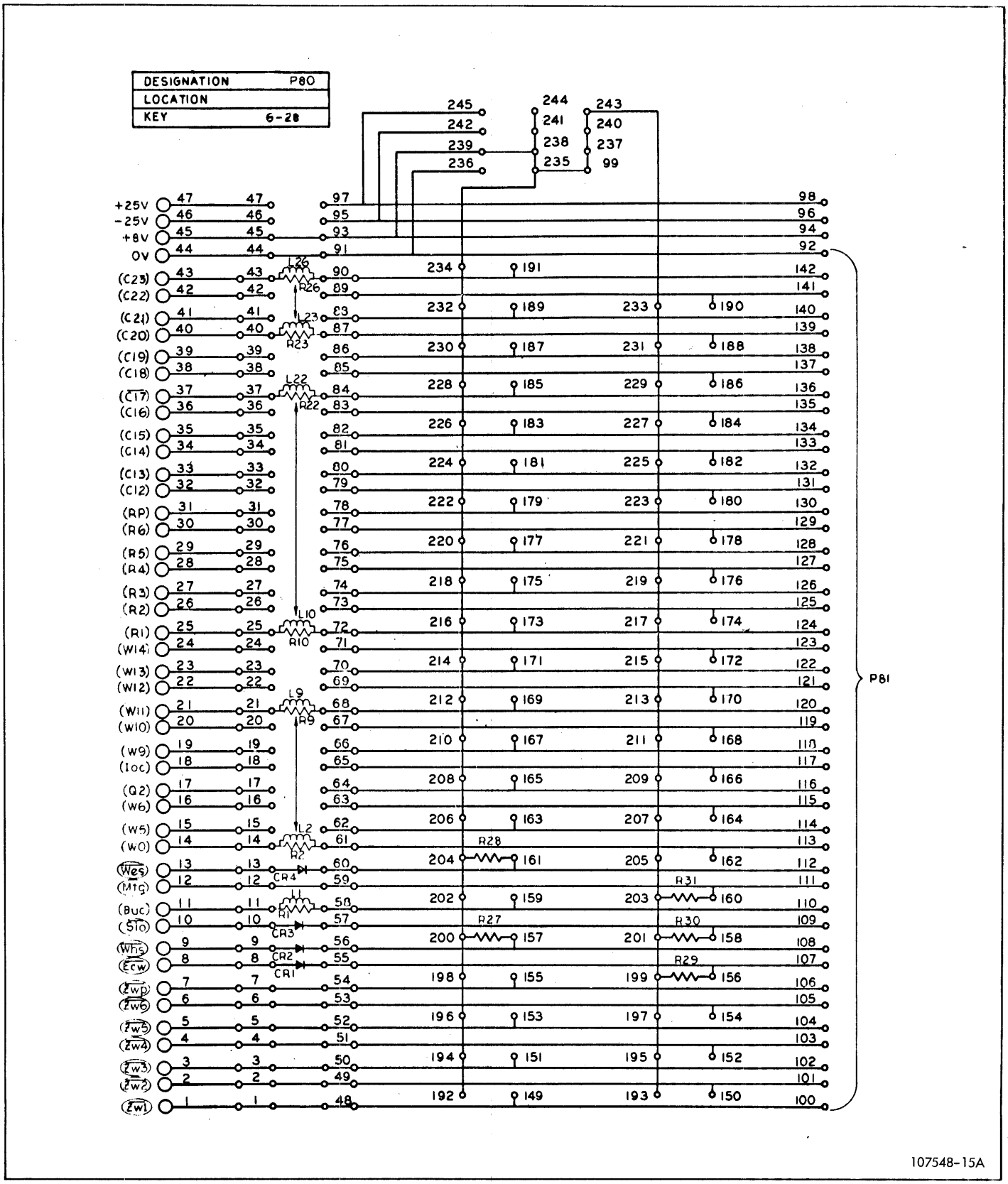


Figure 6-8. Cable Plug Module P80 Schematic Diagram

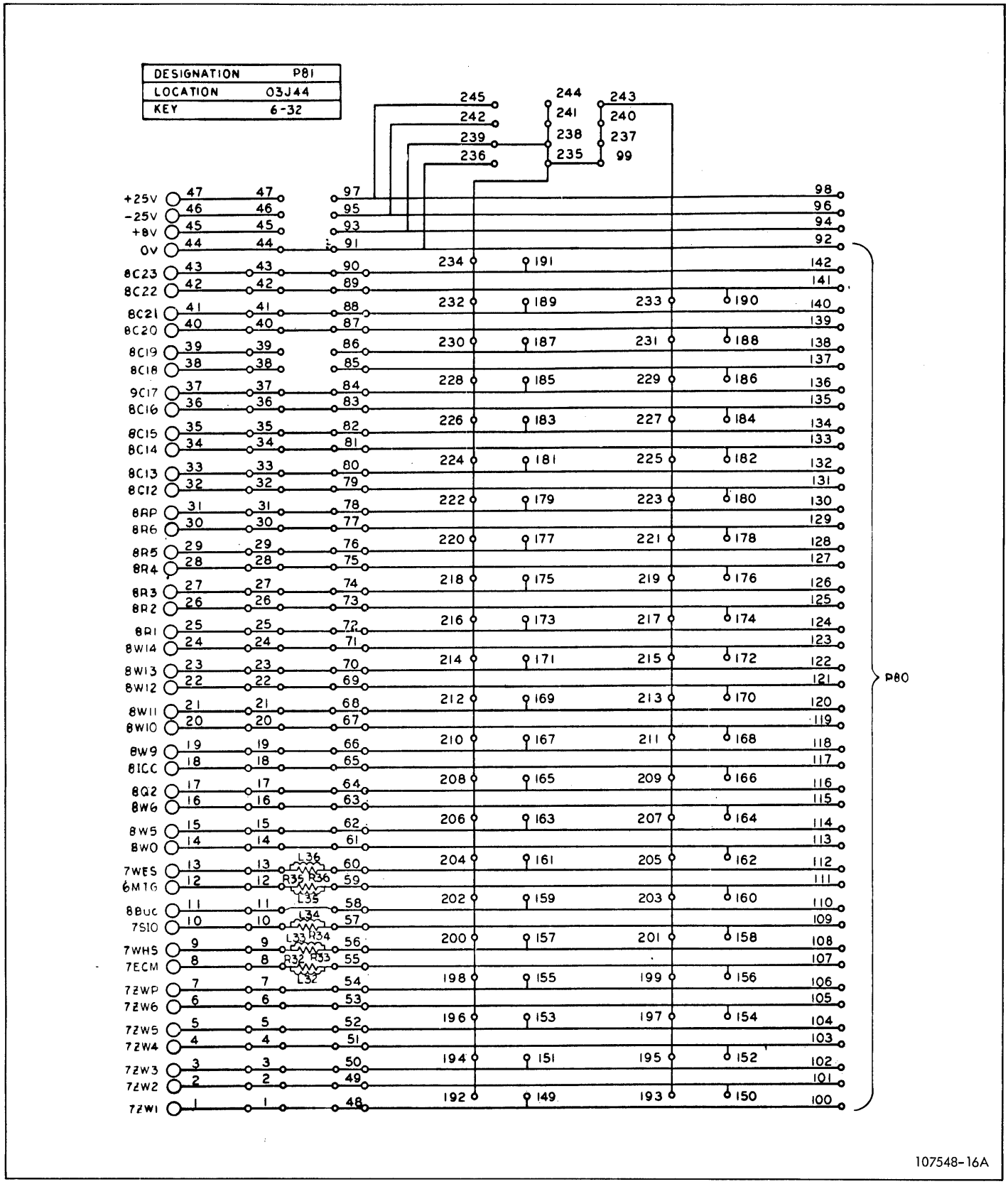


Figure 6-9. Cable Plug Module P81 Schematic Diagram

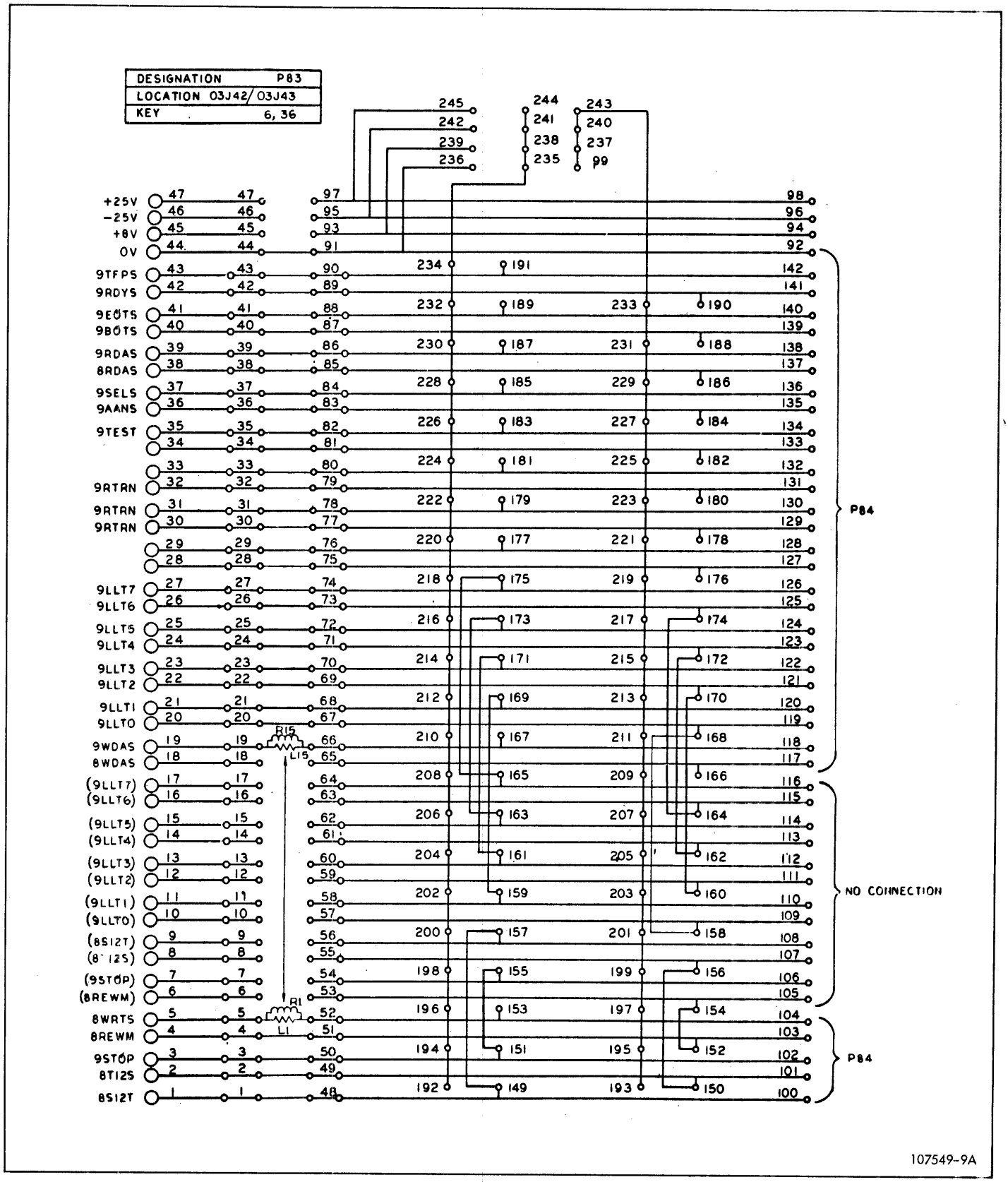


Figure 6-10. Cable Plug Module P83 Schematic Diagram

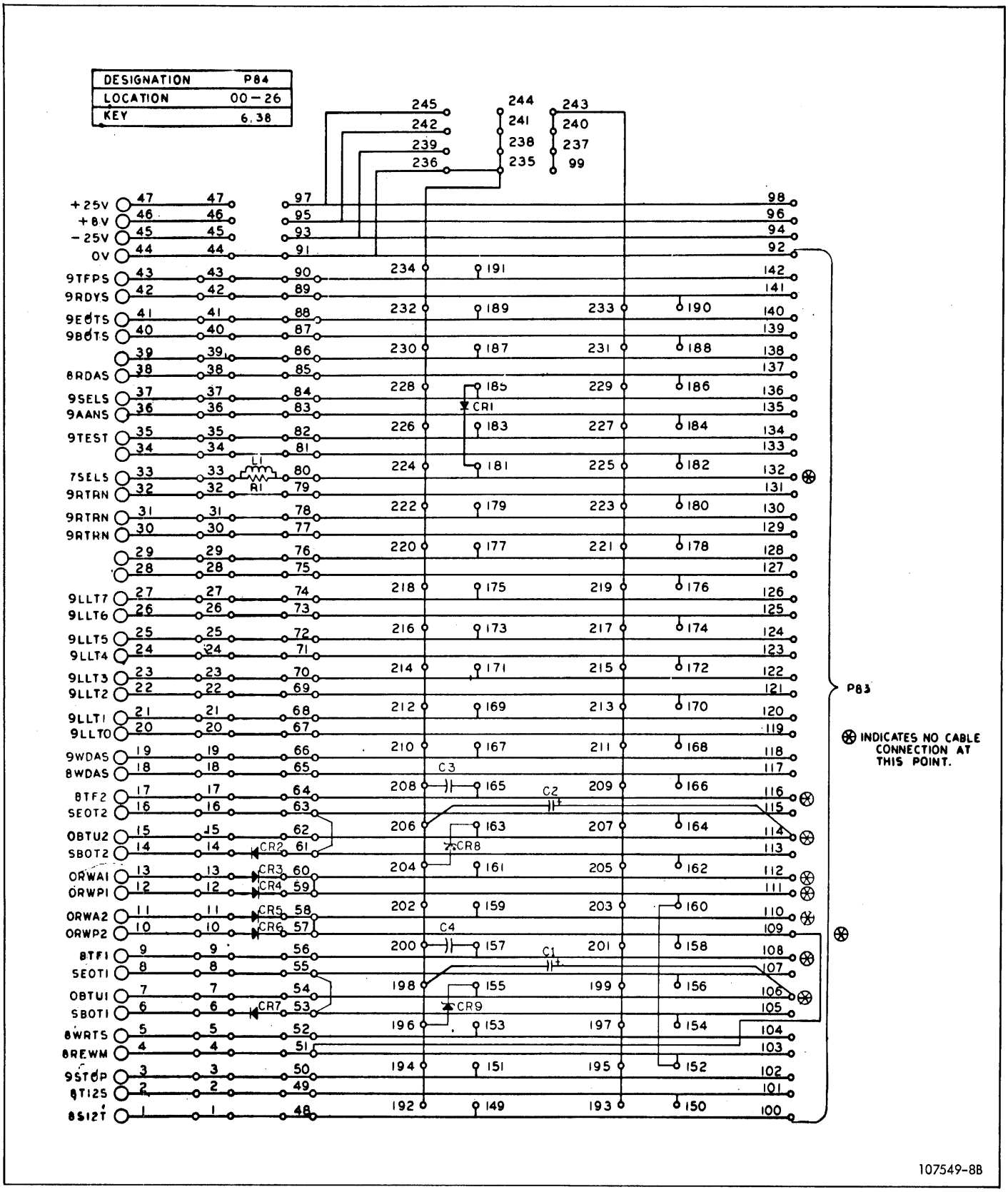


Figure 6-11. Cable Plug Module P84 Schematic Diagram

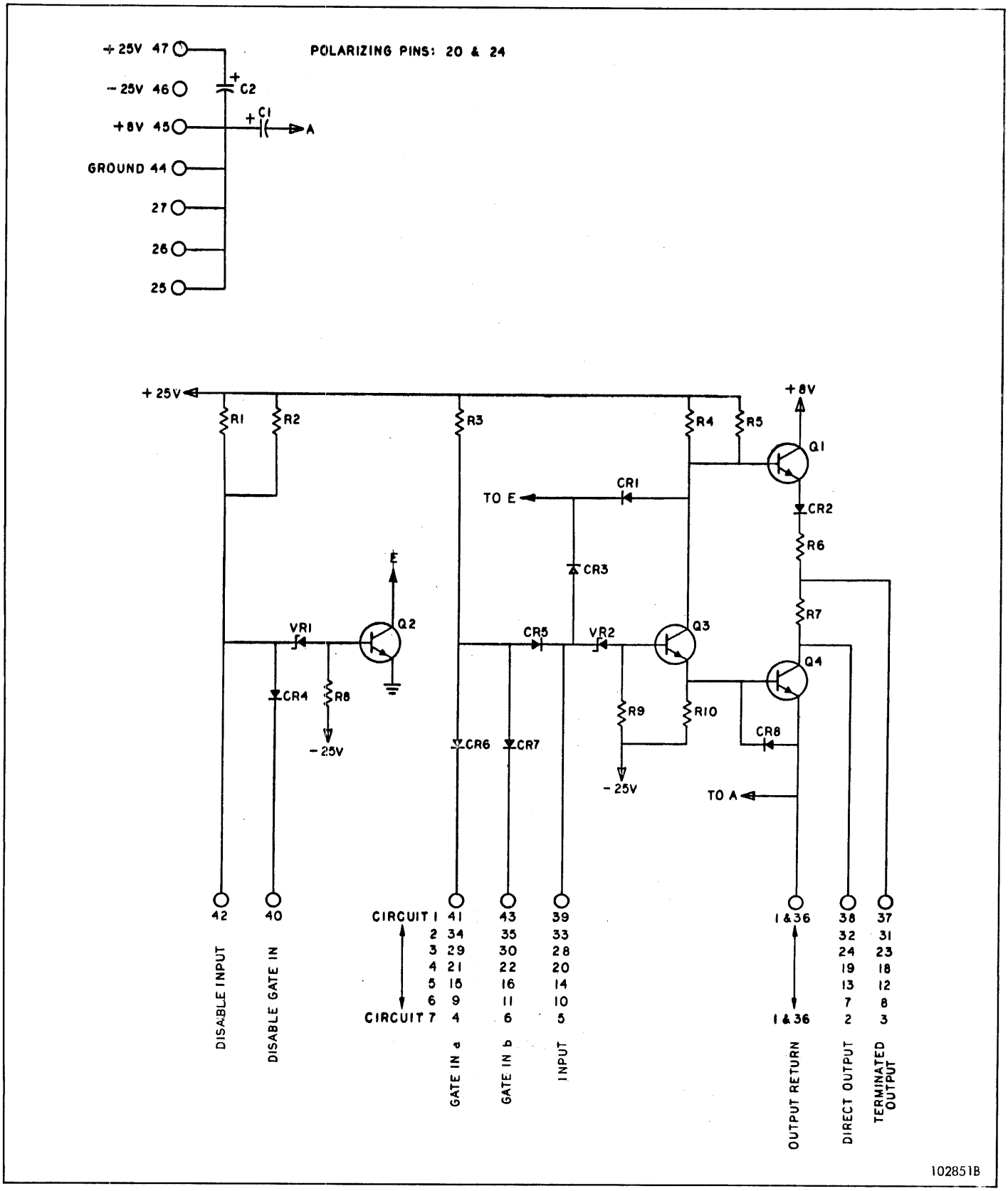
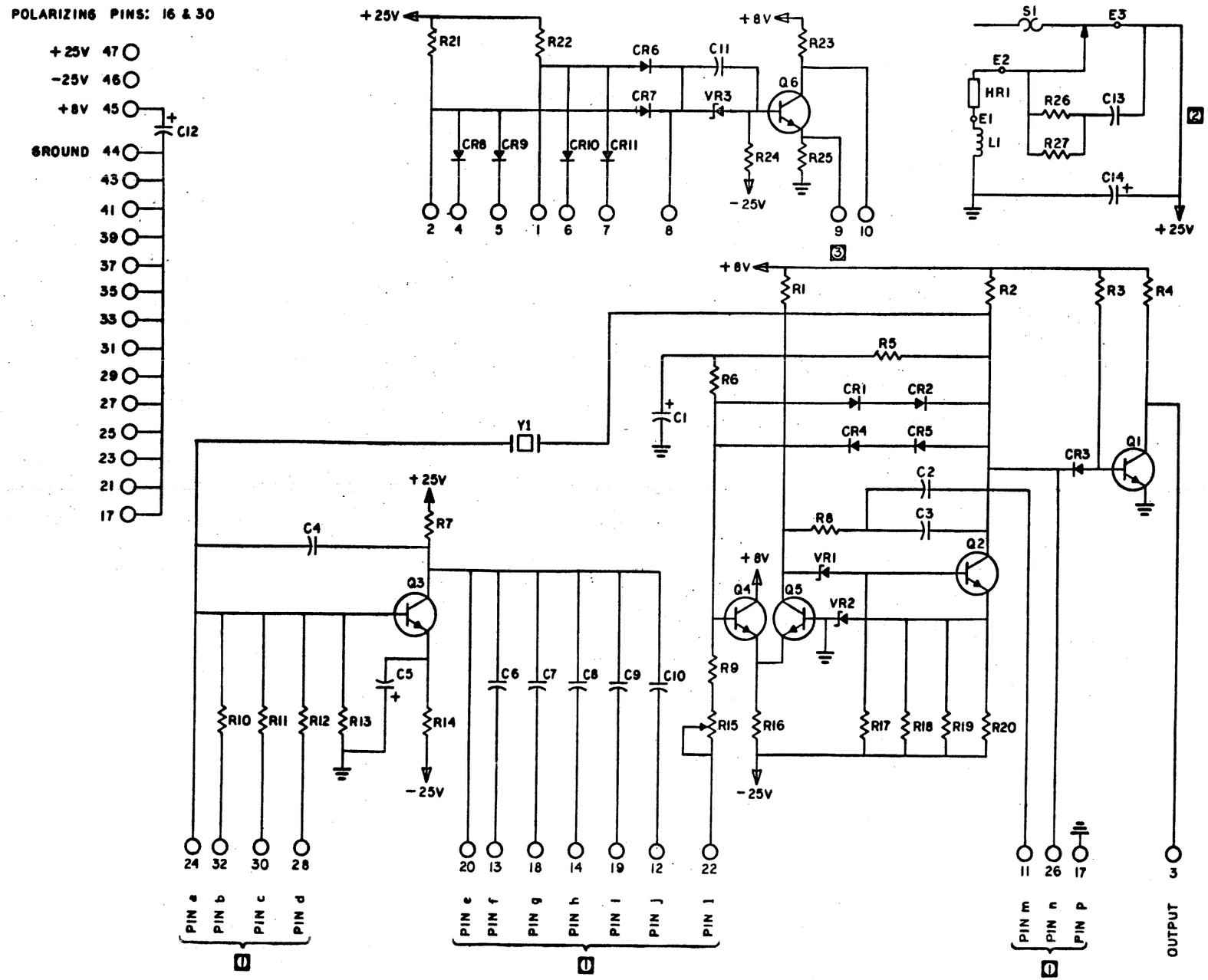


Figure 6-12. Cable Driver AX14 Schematic Diagram



NOTES:

1. THE TABLE BELOW LISTS PIN CONNECTIONS TO BE MADE DEPENDING UPON THE FREQUENCY OF THE CRYSTAL USED.

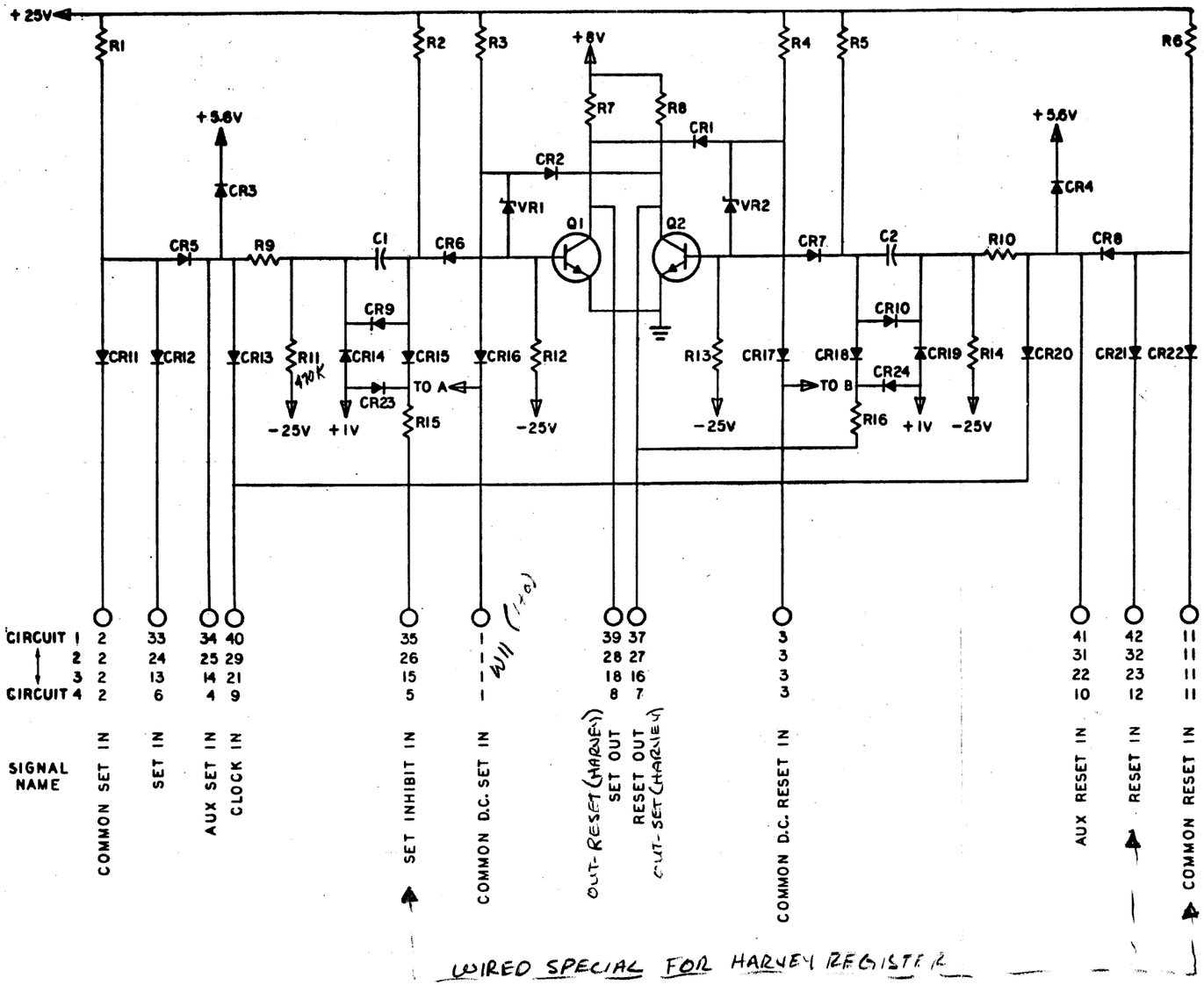
CRYSTAL FREQUENCY RANGE	PIN CONNECTIONS											
	b	c	d	f	g	h	i	j	l	m	n	p
1 MC TO 300 KC	X					X						
					X				X			
300 KC TO 100 KC		X		X								
						X			X			
										X		X
100 KC TO 30 KC			X	X								
							X		X			
										X		X
30 KC TO 10 KC			X			X						
							X				X	
								X	X			
										X		X

2. OVEN ASSEMBLY IS OMITTED ON CX13.
3. IF OUTPUT PIN #10 IS USED AS CLOCK FOR FLIP-FLOPS, PIN #9 SHOULD BE GROUNDED NEAR THE FLIP FLOPS; OTHERWISE IT MAY BE GROUNDED LOCALLY.
4. OVEN COVER SHIELD IS SAME AS GROUND FOR CX14.

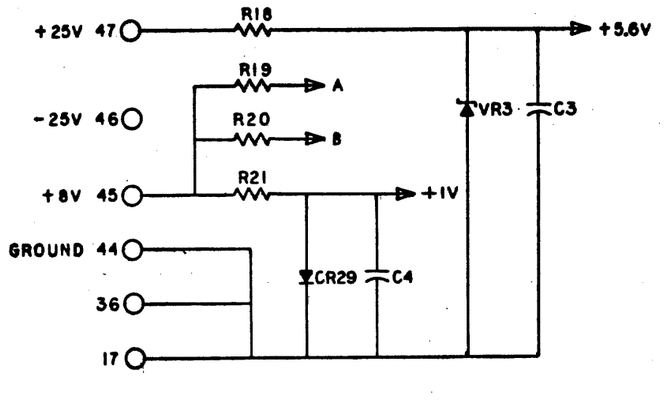
Figure 6-13. Crystal Clock Generator CX13 Schematic Diagram

102169D

PIN 35 = 1 = ONLY SET
PIN 35 = 0 = ONLY RESET



POLARIZING PINS: 8 & 30



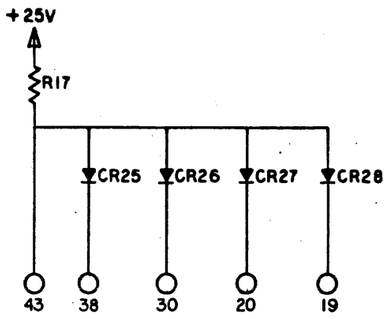


Figure 6-14. Counter Flip-Flop FH15 Schematic Diagram

101002B

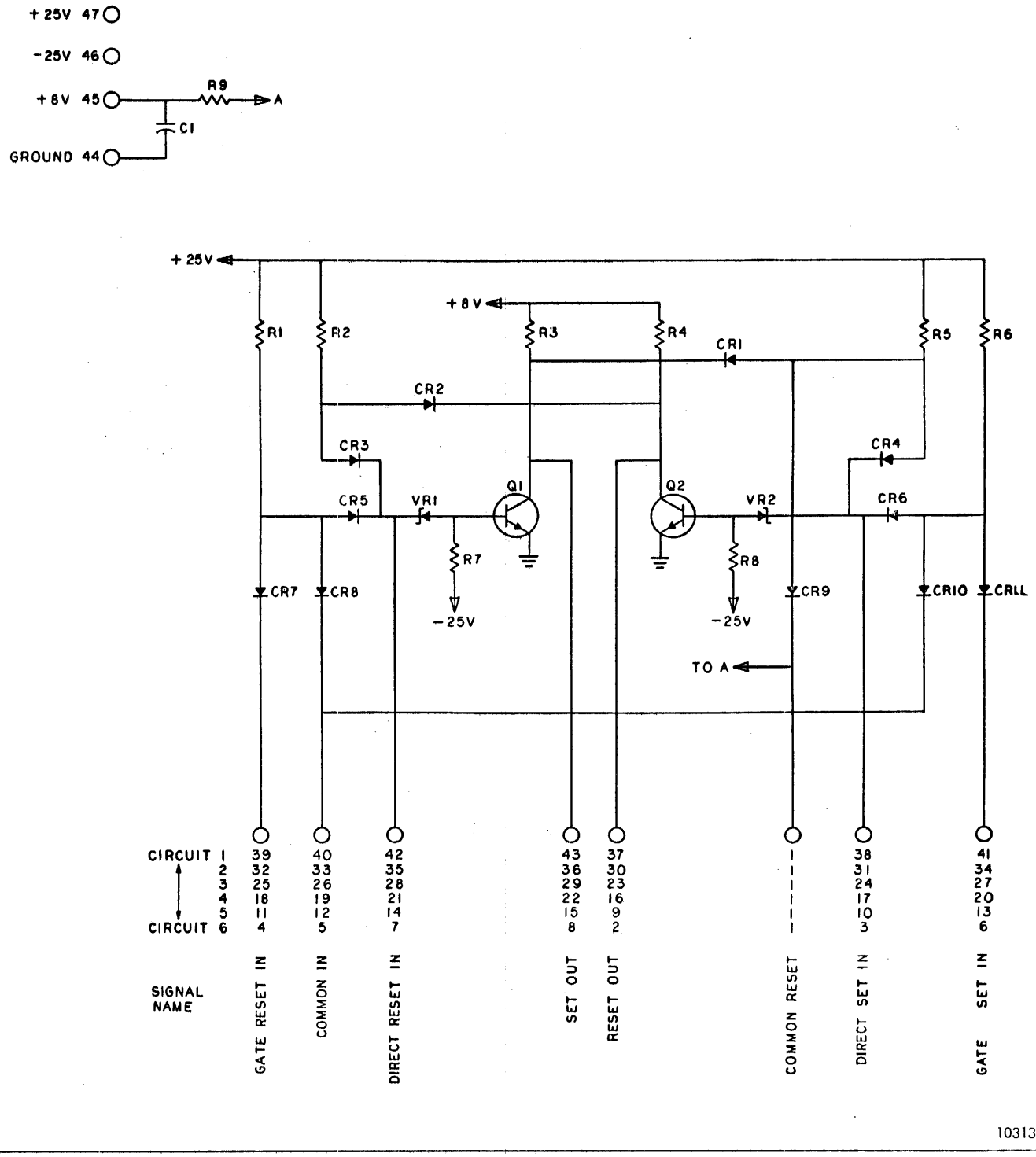


Figure 6-15. DC Flip-Flop FH19 Schematic Diagram

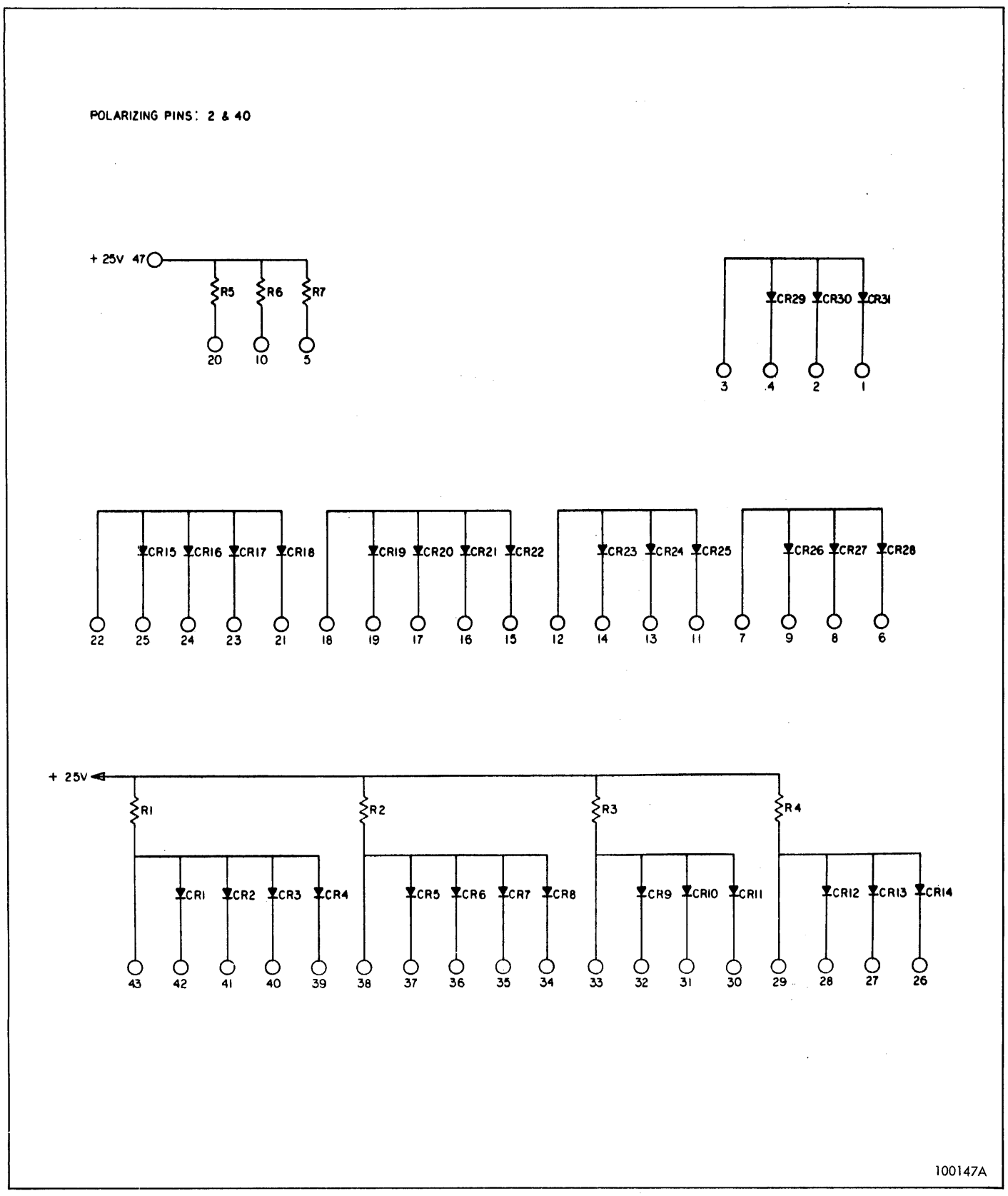


Figure 6-16. Gate Expander GH10 Schematic Diagram

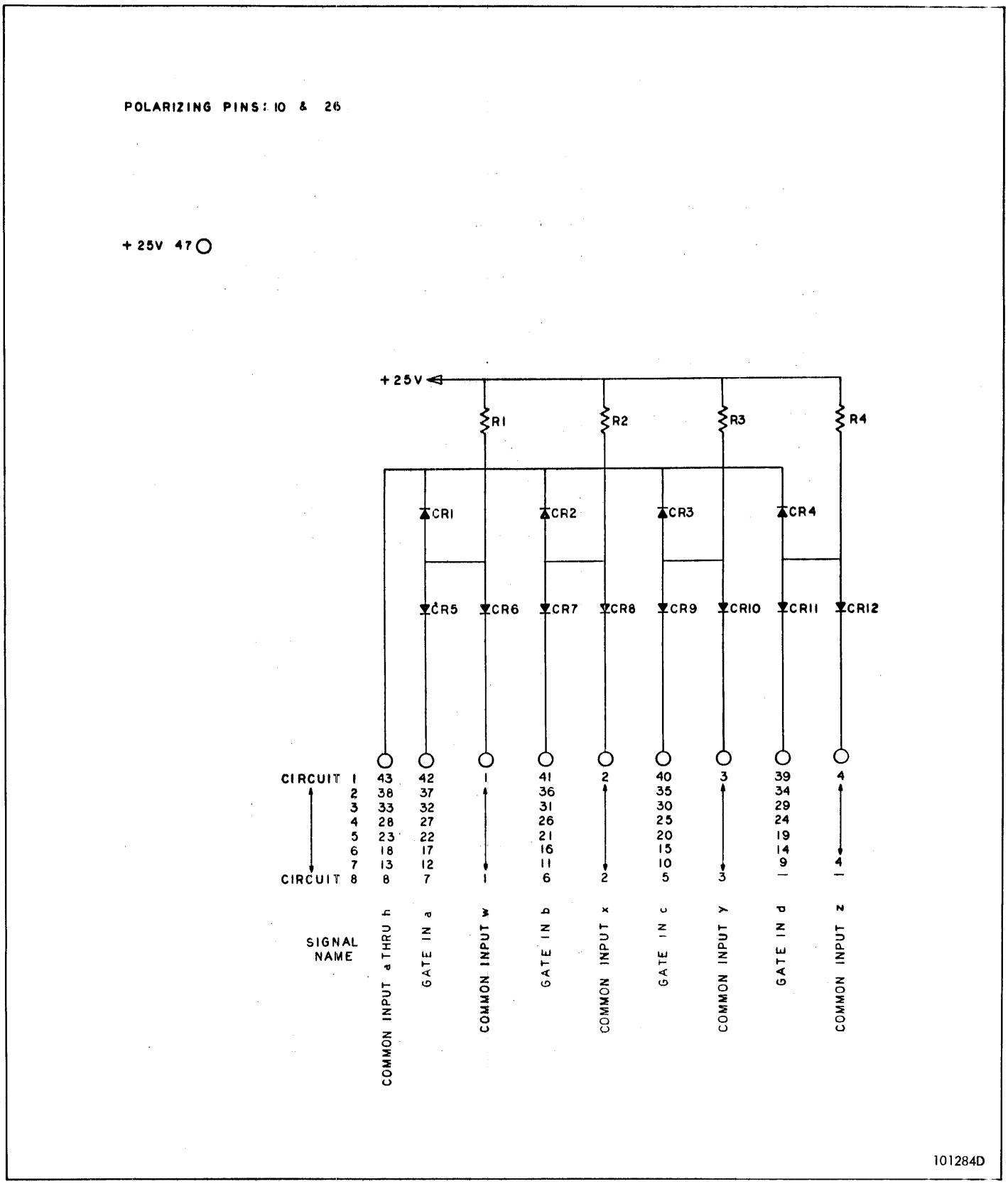


Figure 6-17. Gate Expander GH11 Schematic Diagram

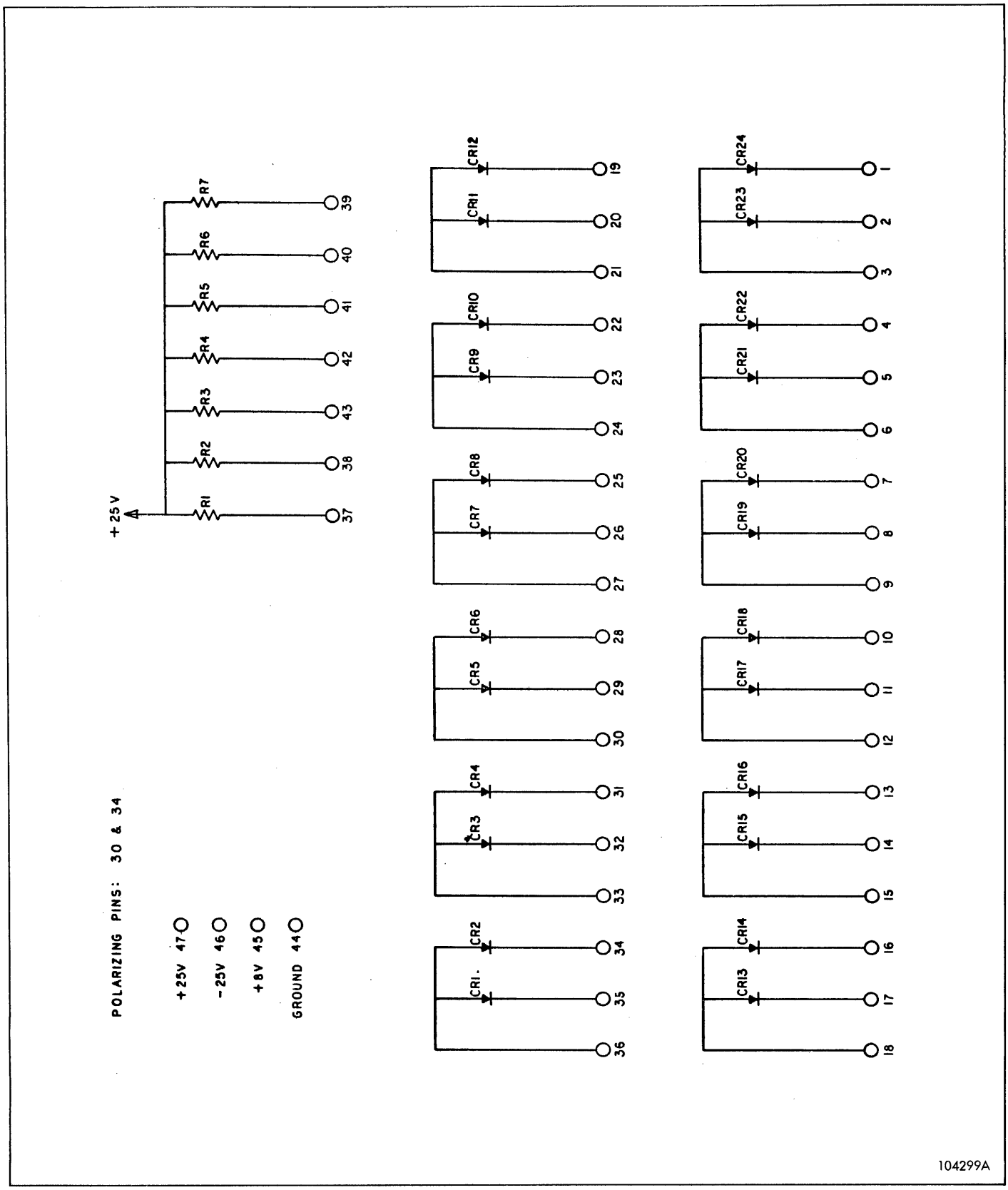


Figure 6-18. Gate Expander GH14 Schematic Diagram

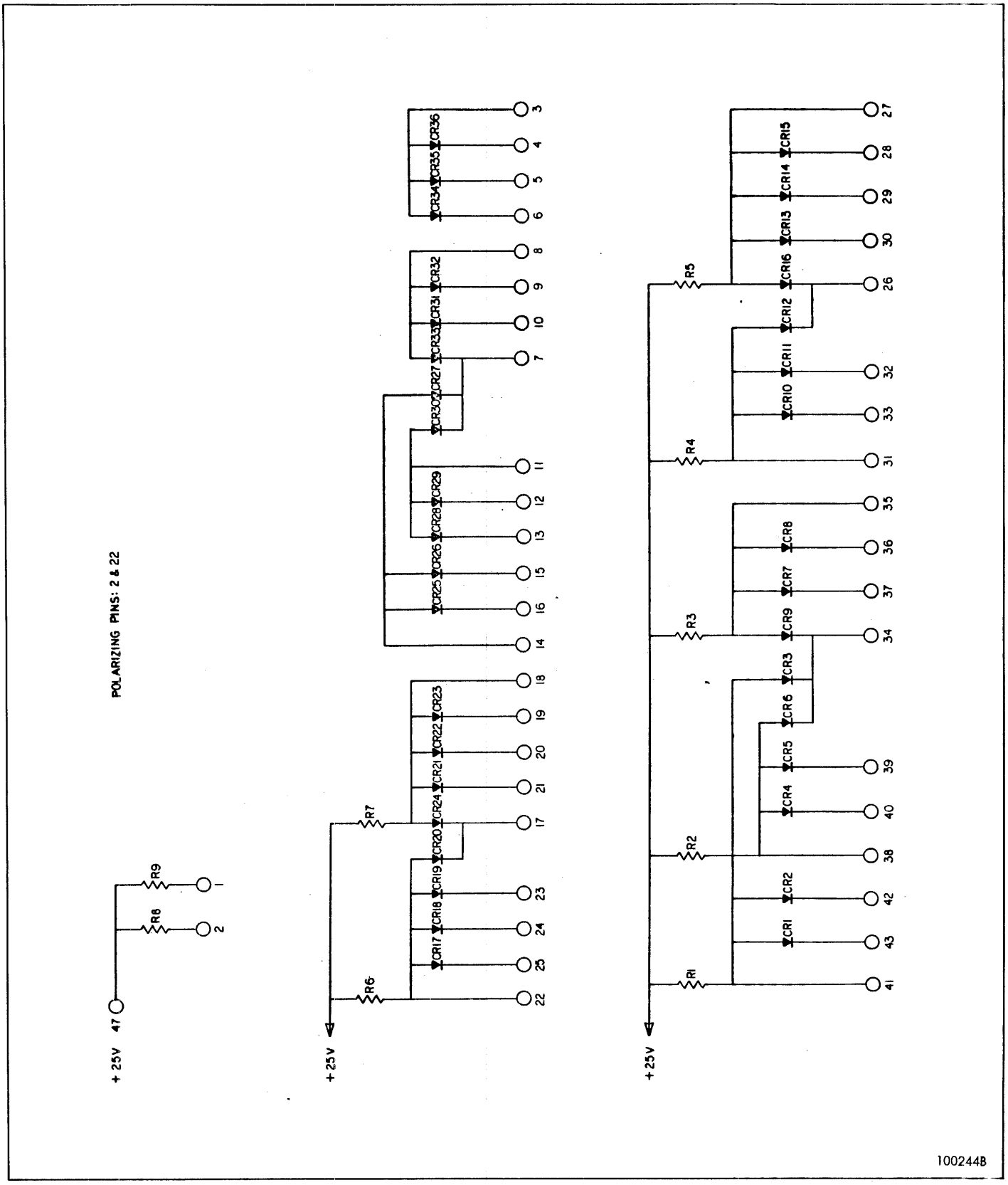


Figure 6-19. Diode Gate No. 1 GK51 Schematic Diagram

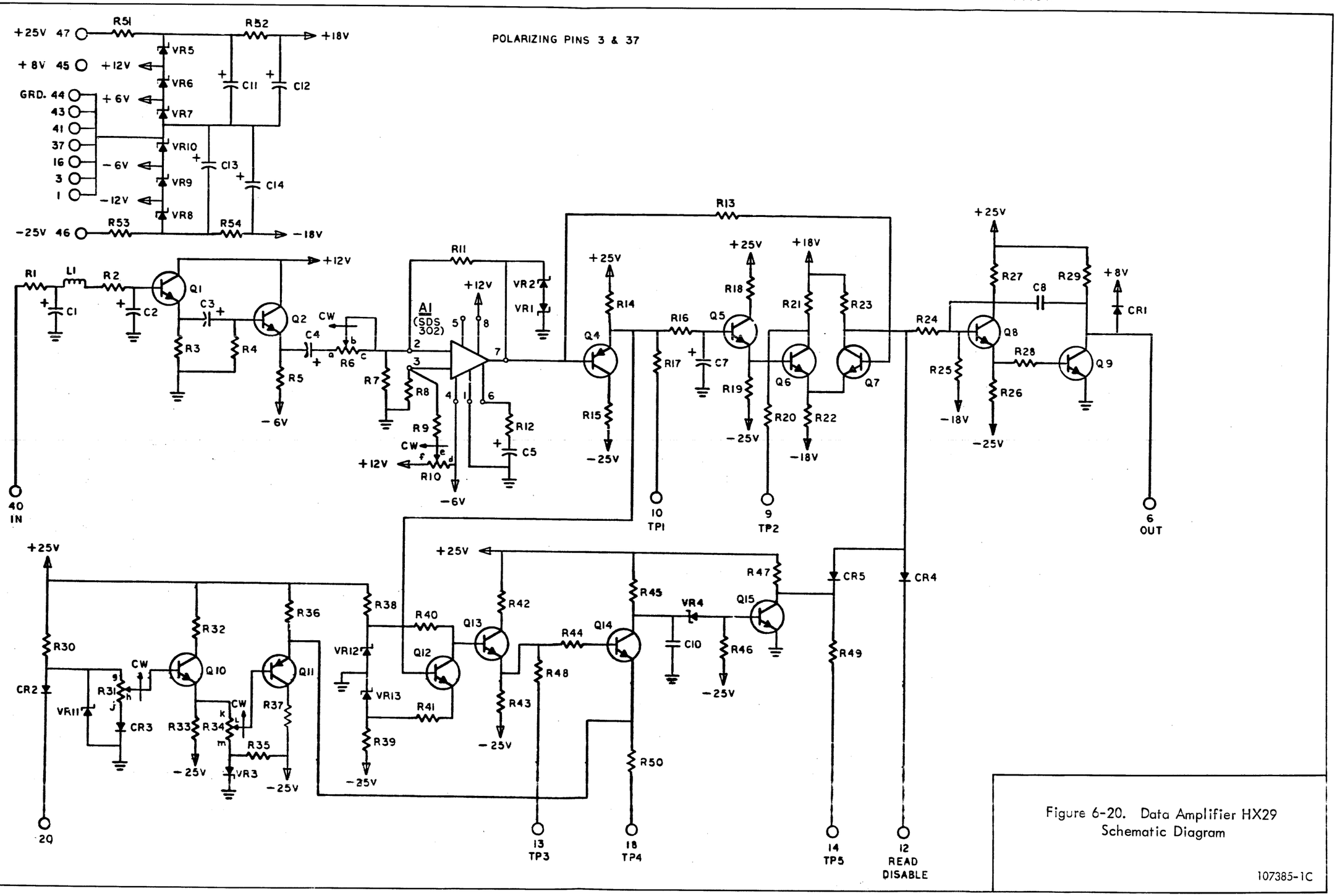


Figure 6-20. Data Amplifier HX29 Schematic Diagram

107385-1C

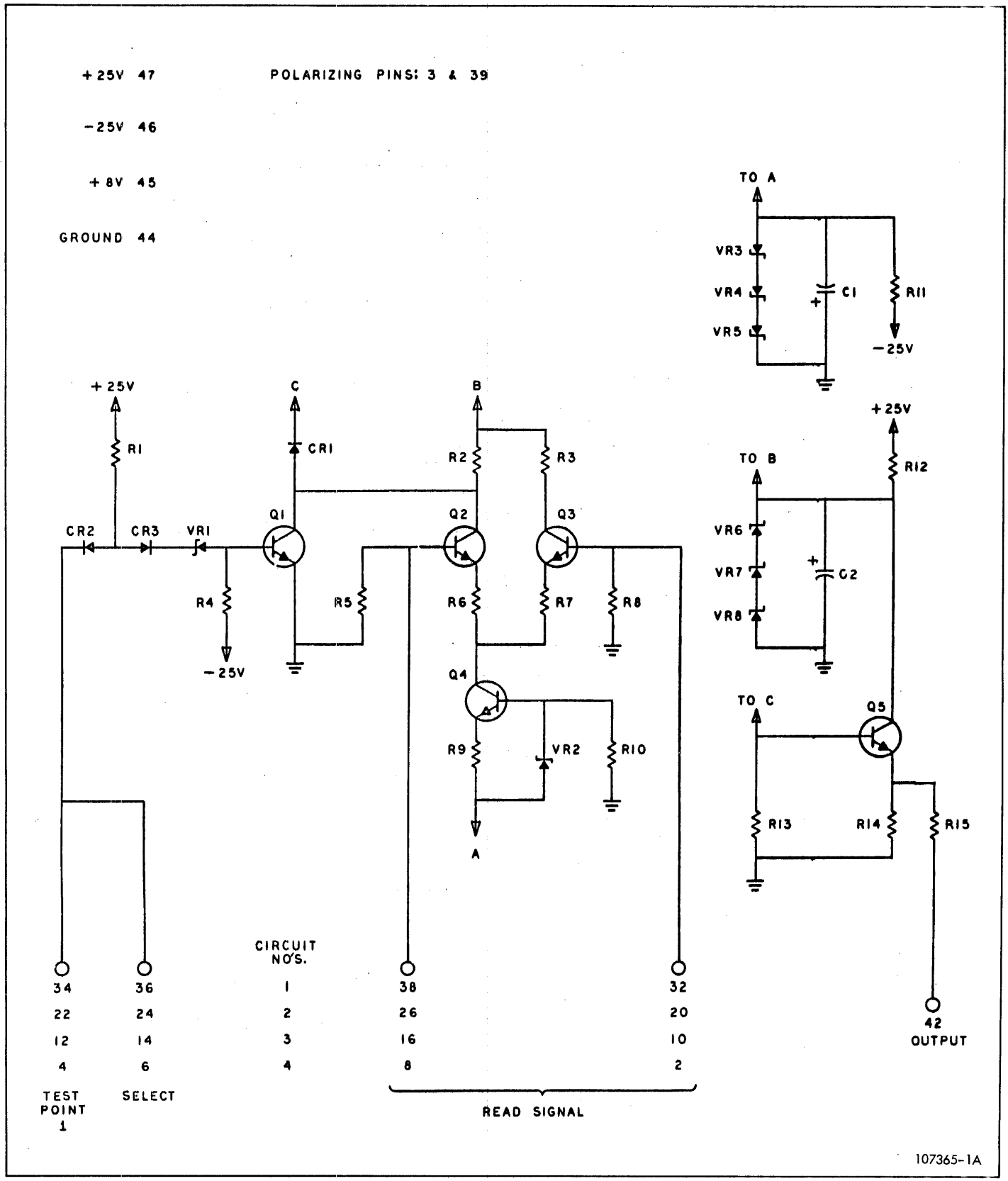


Figure 6-21. Gated Read Amplifier HX30 Schematic Diagram

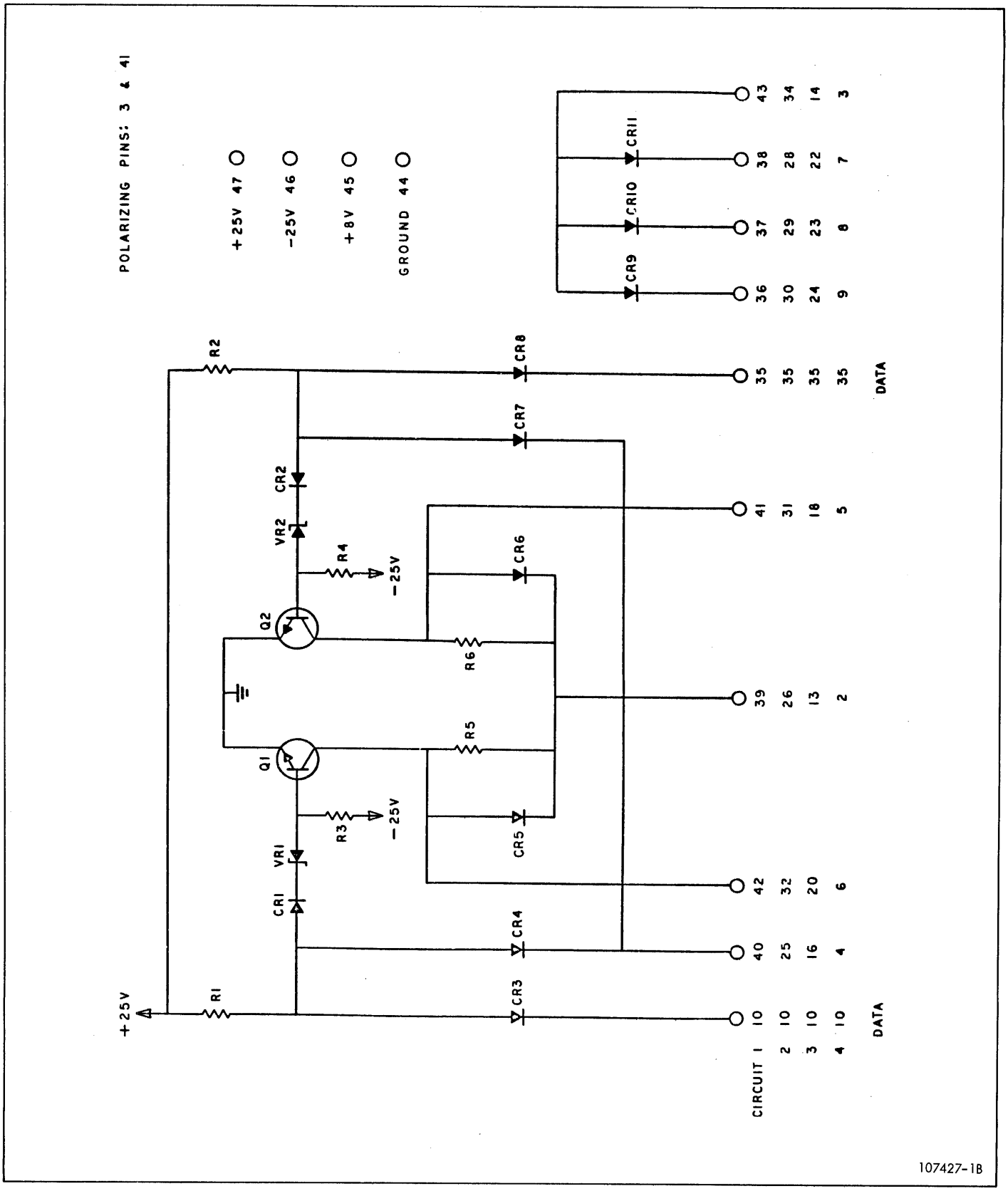


Figure 6-22. Gated Write Amplifier HX31 Schematic Diagram

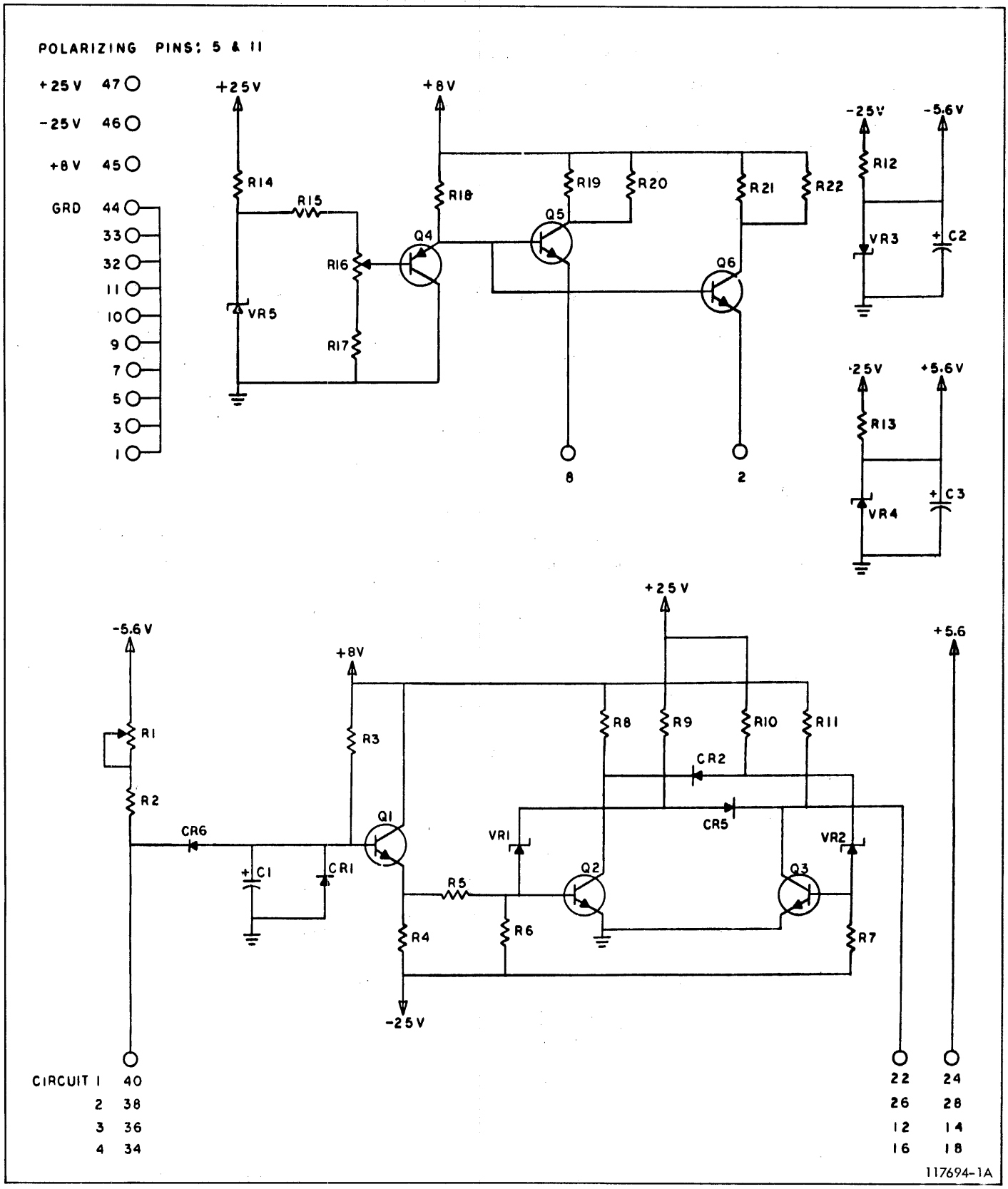


Figure 6-23. Delayed Photosense Amplifier HX48 Schematic Diagram

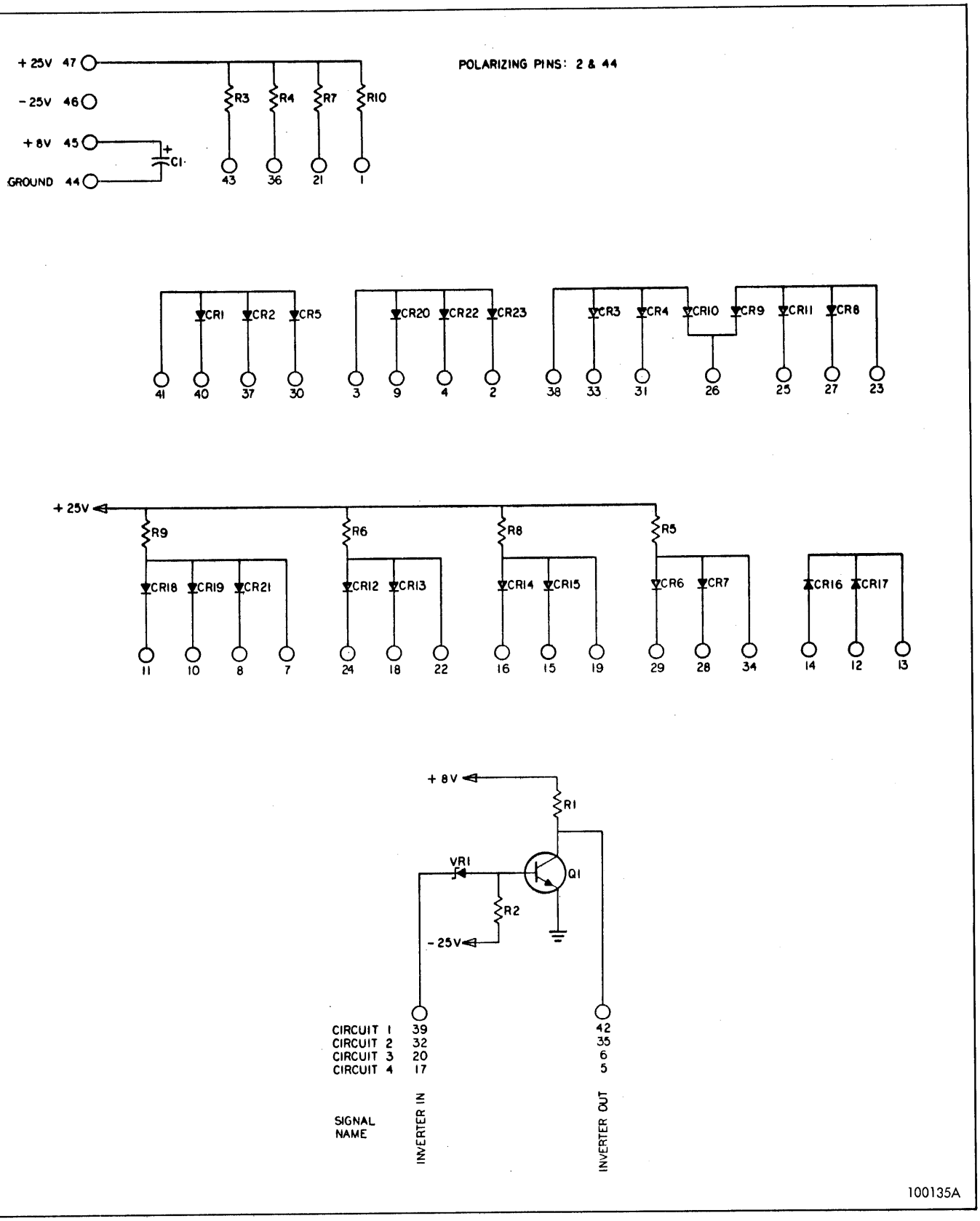


Figure 6-24. AND/OR Inverter IH10 Schematic Diagram

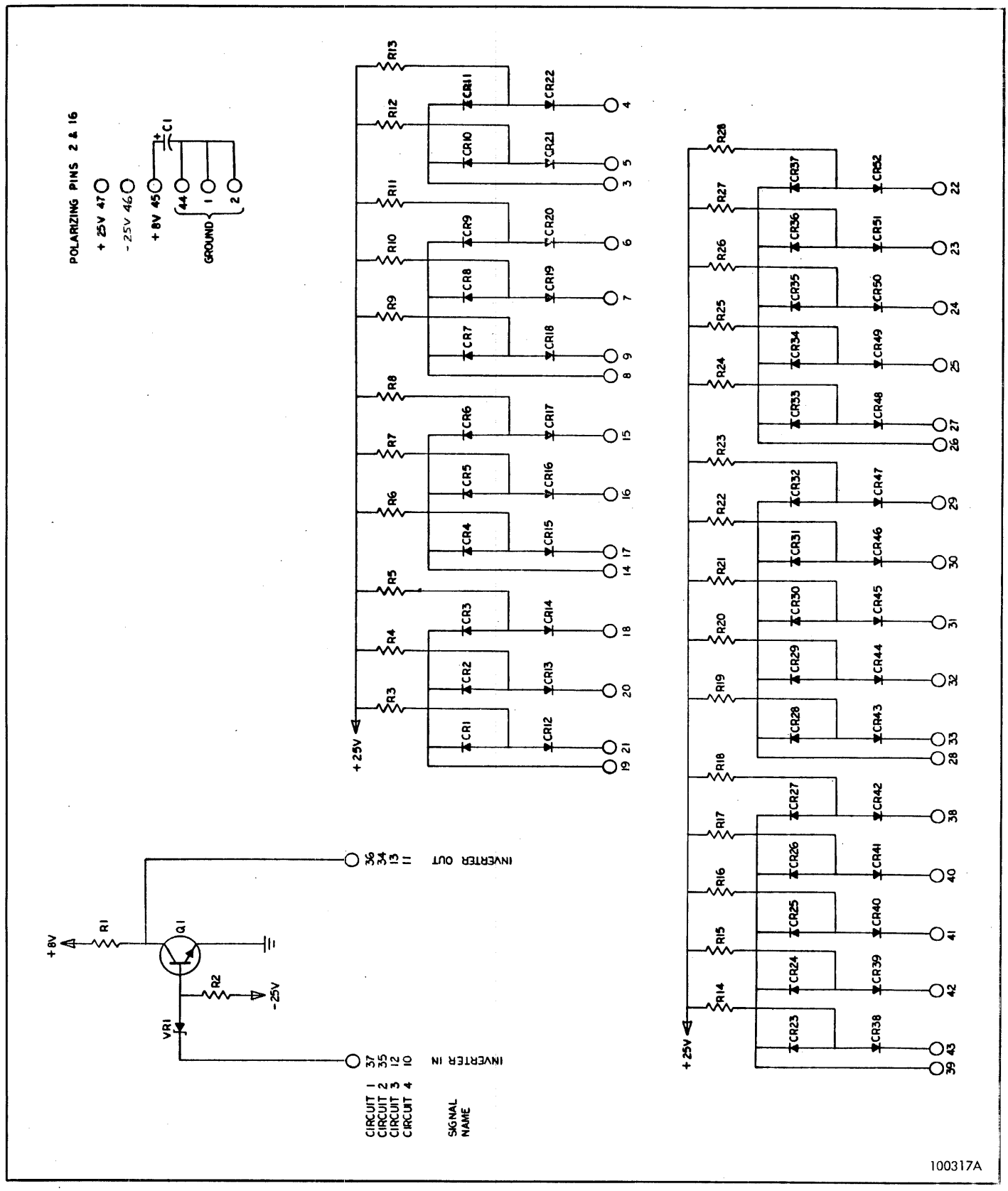


Figure 6-25. OR Gate Inverter IH11 Schematic Diagram

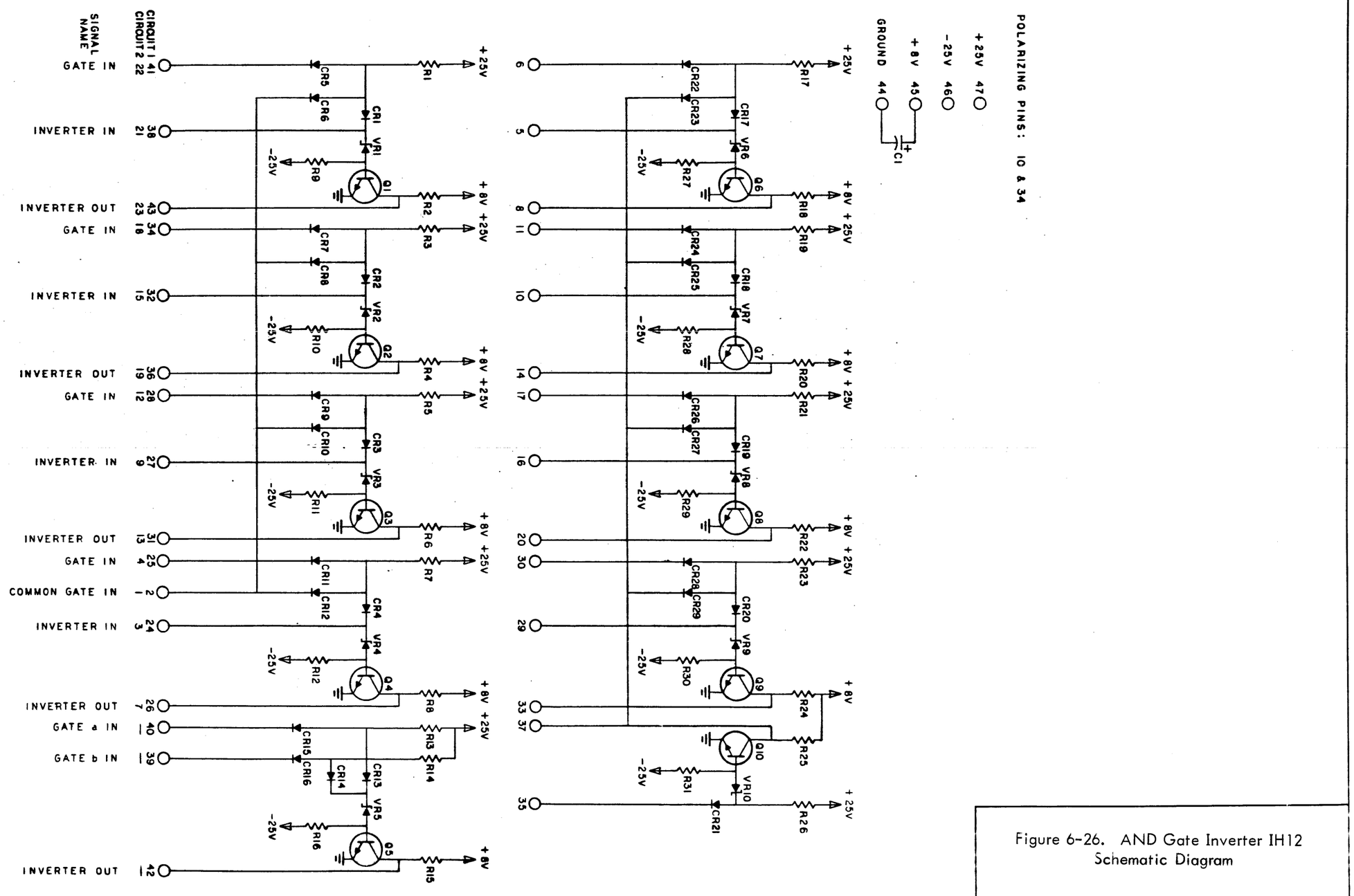


Figure 6-26. AND Gate Inverter IH12 Schematic Diagram

101538B

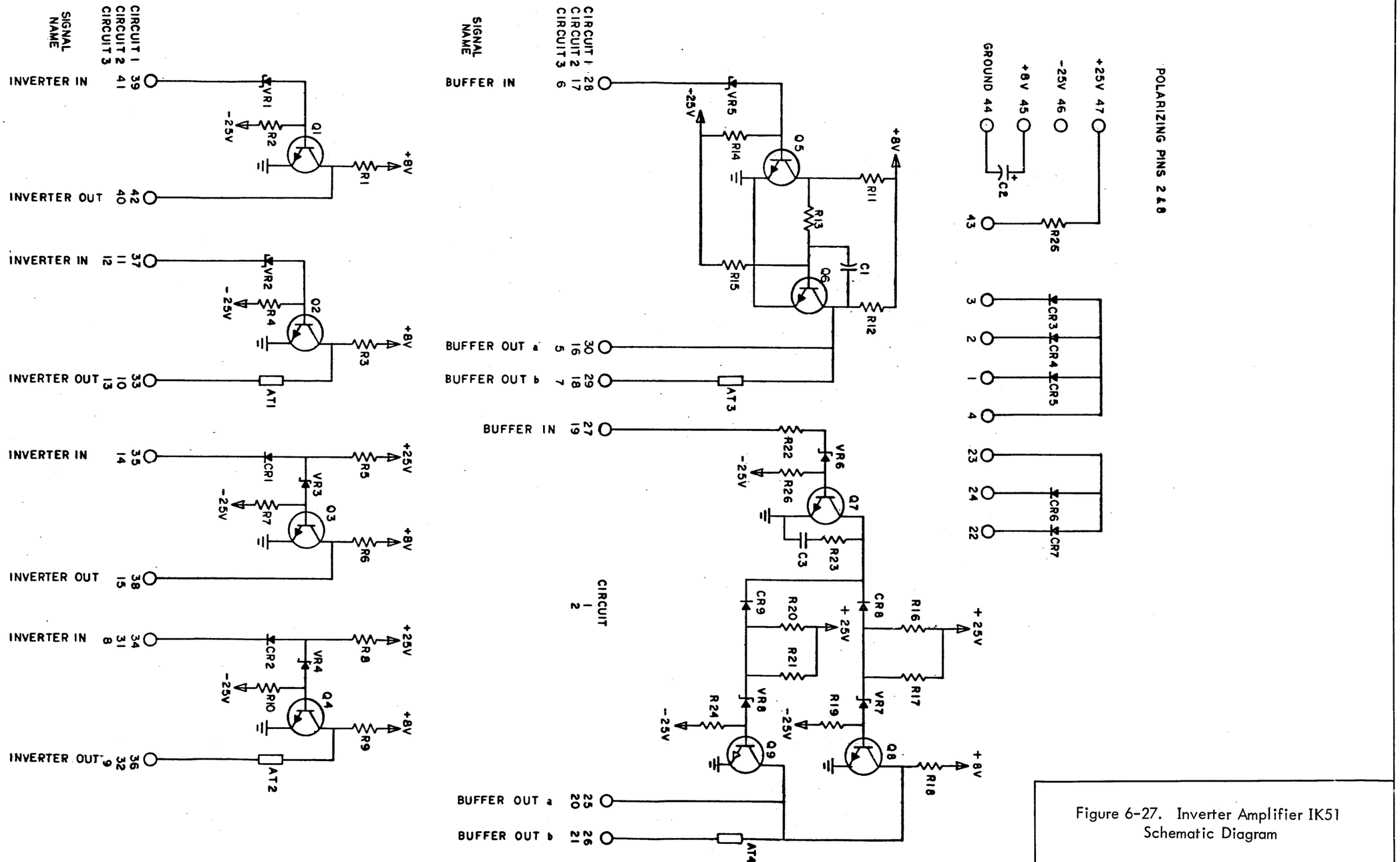


Figure 6-27. Inverter Amplifier IK51 Schematic Diagram

100386H

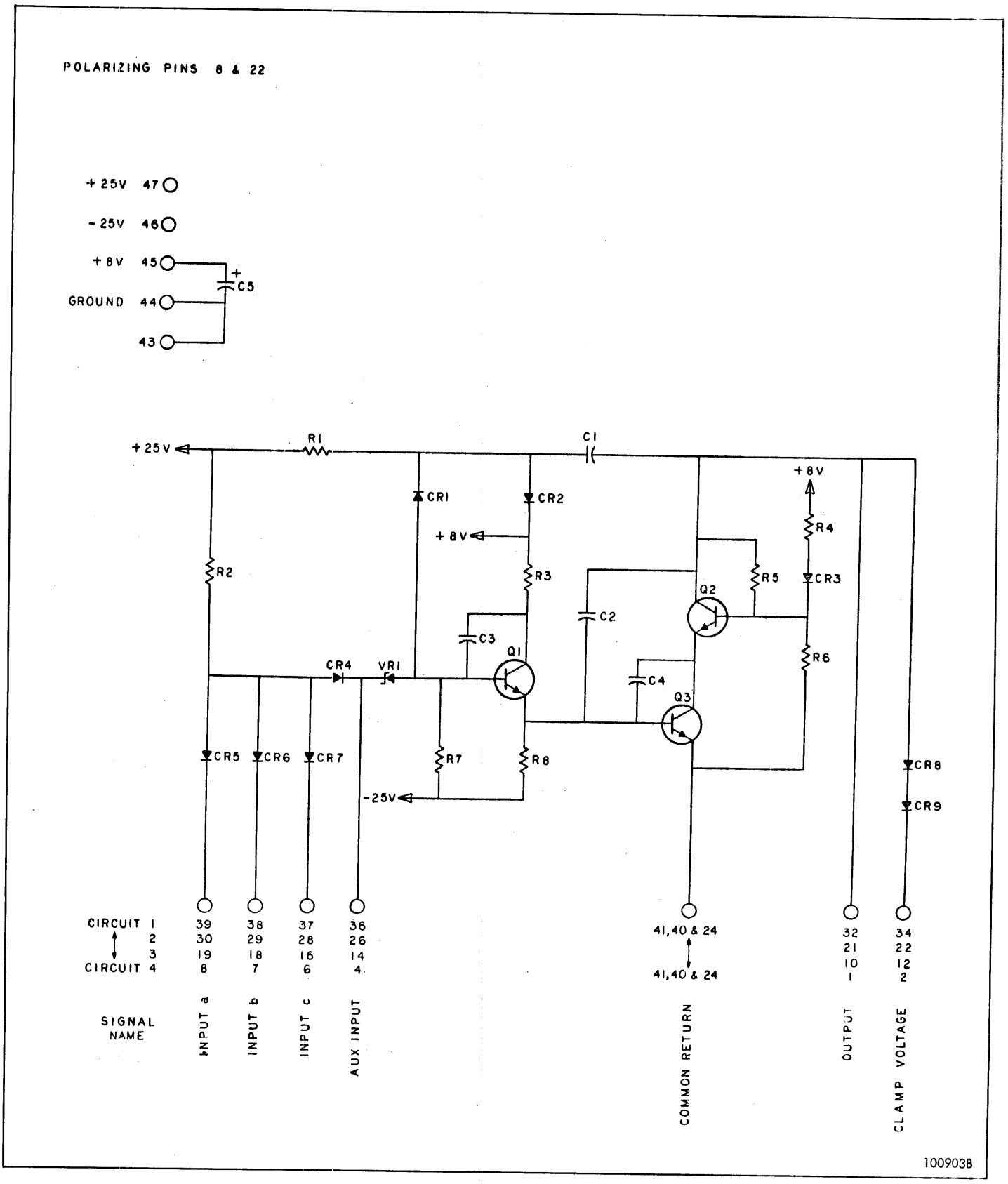


Figure 6-28. Relay Driver RK53 Schematic Diagram

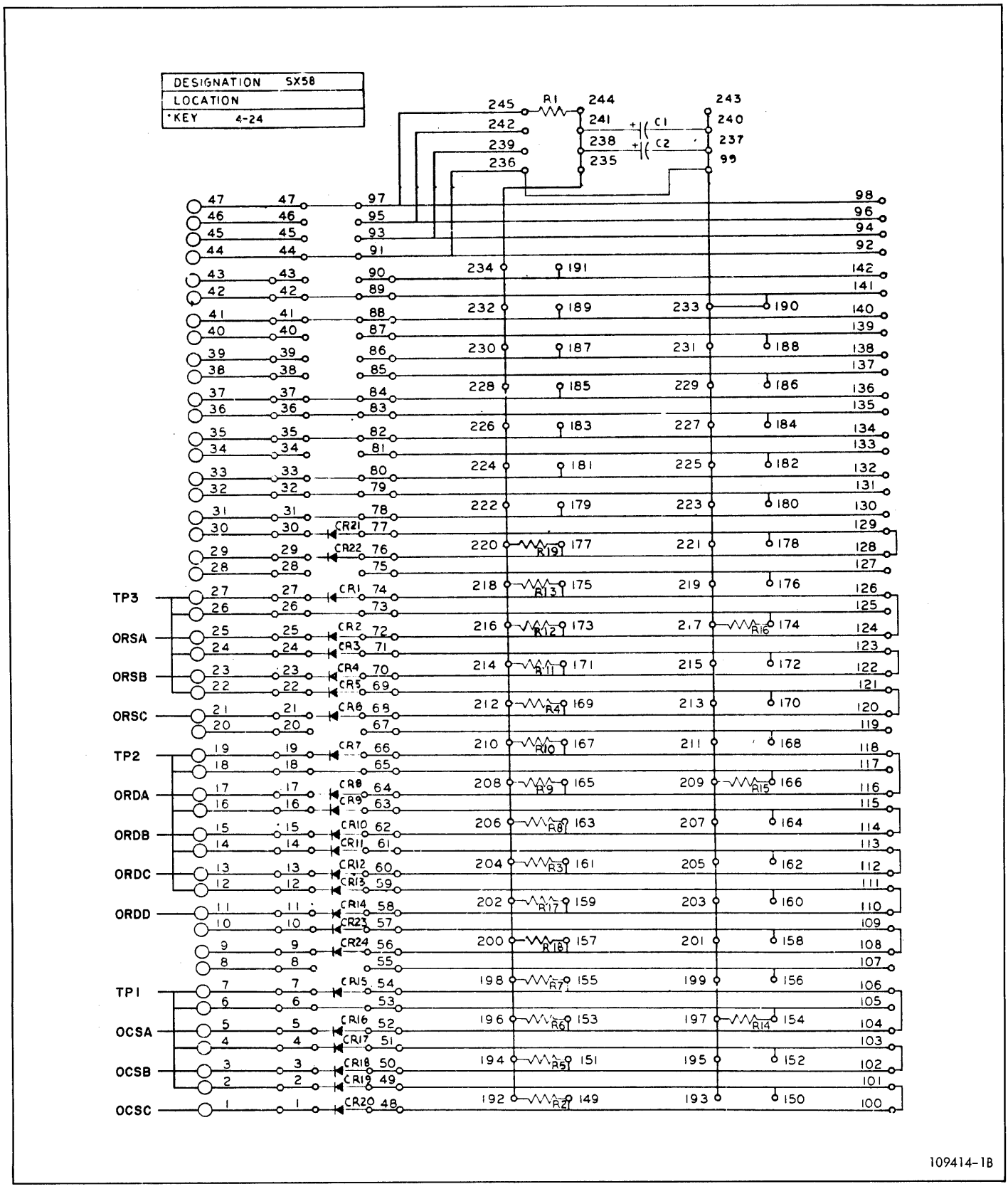


Figure 6-29. Digital-to-Staircase Converter SX58 Schematic Diagram

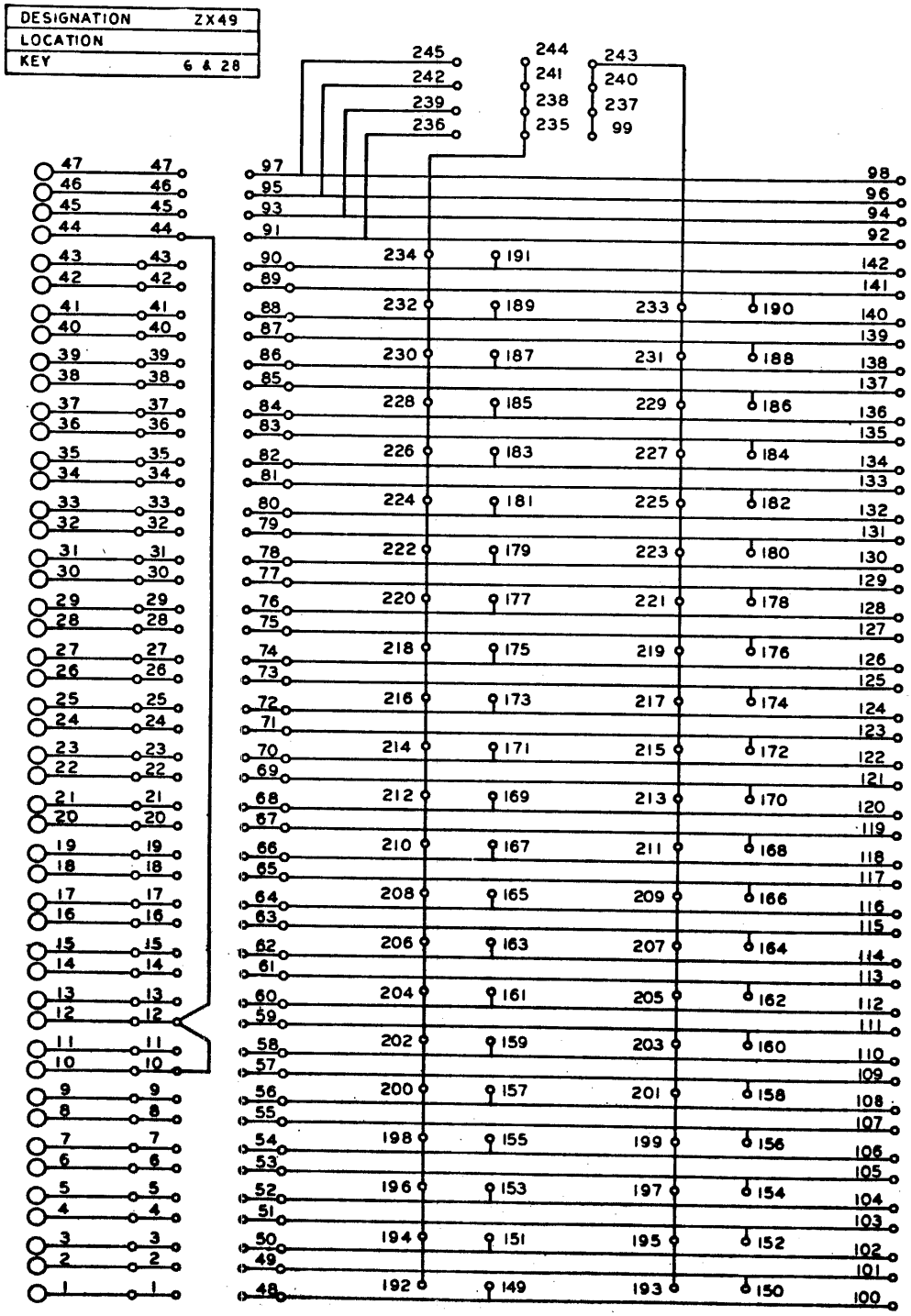


Figure 6-30. Termination Module ZX49 Schematic Diagram